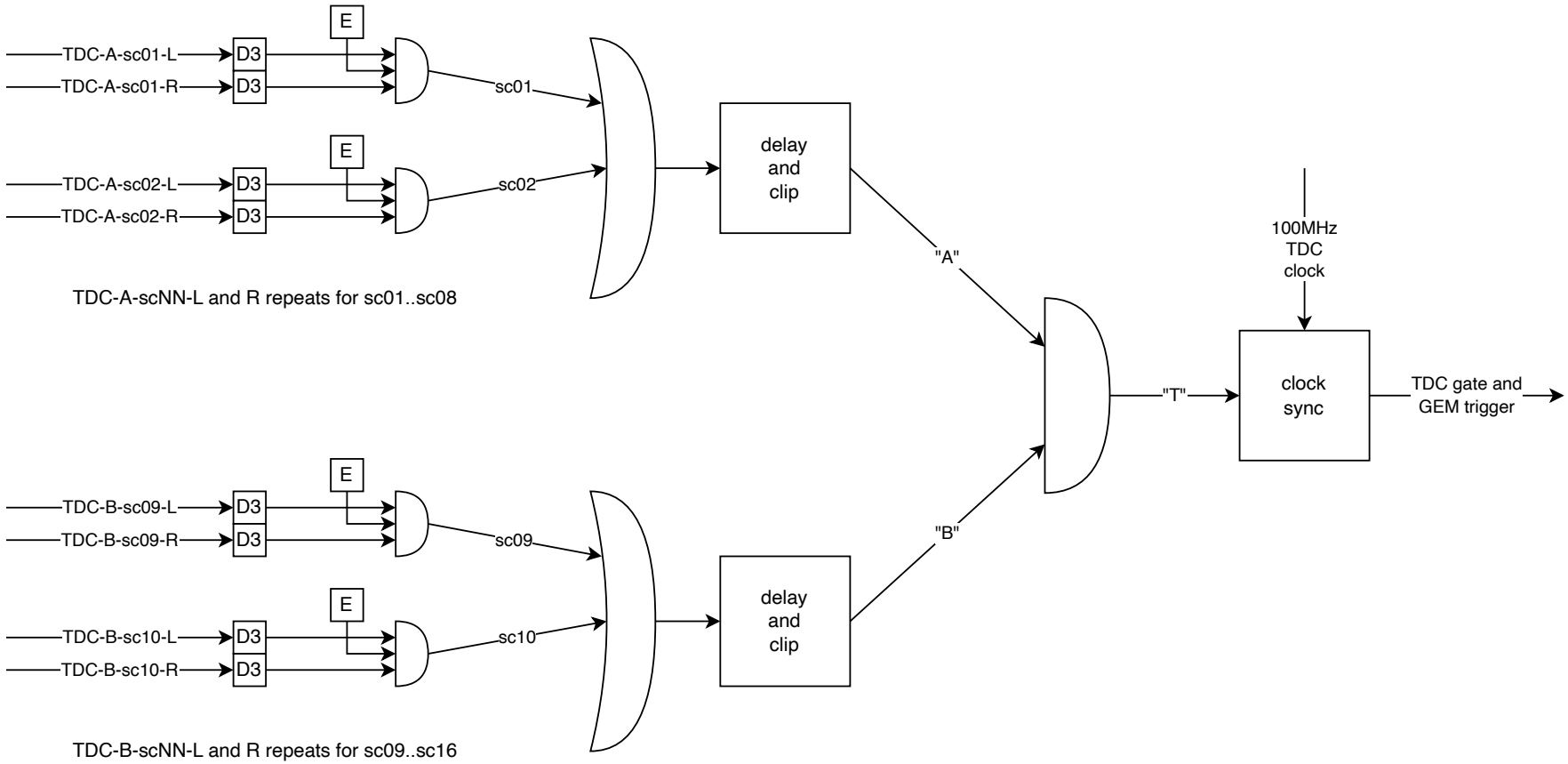
DarkLight FPGA trigger logic, 21-July-2025, K.O.



Notes:

"D3" is the FPGA input pin delay, 7 steps of 0.3 ns, set at compile time
"E" is the "trigger enable" bits from ODB dl_trg_mask
"delay and clip" will be constructed from discrete logic to time the electron-position coincidence, set at compile time