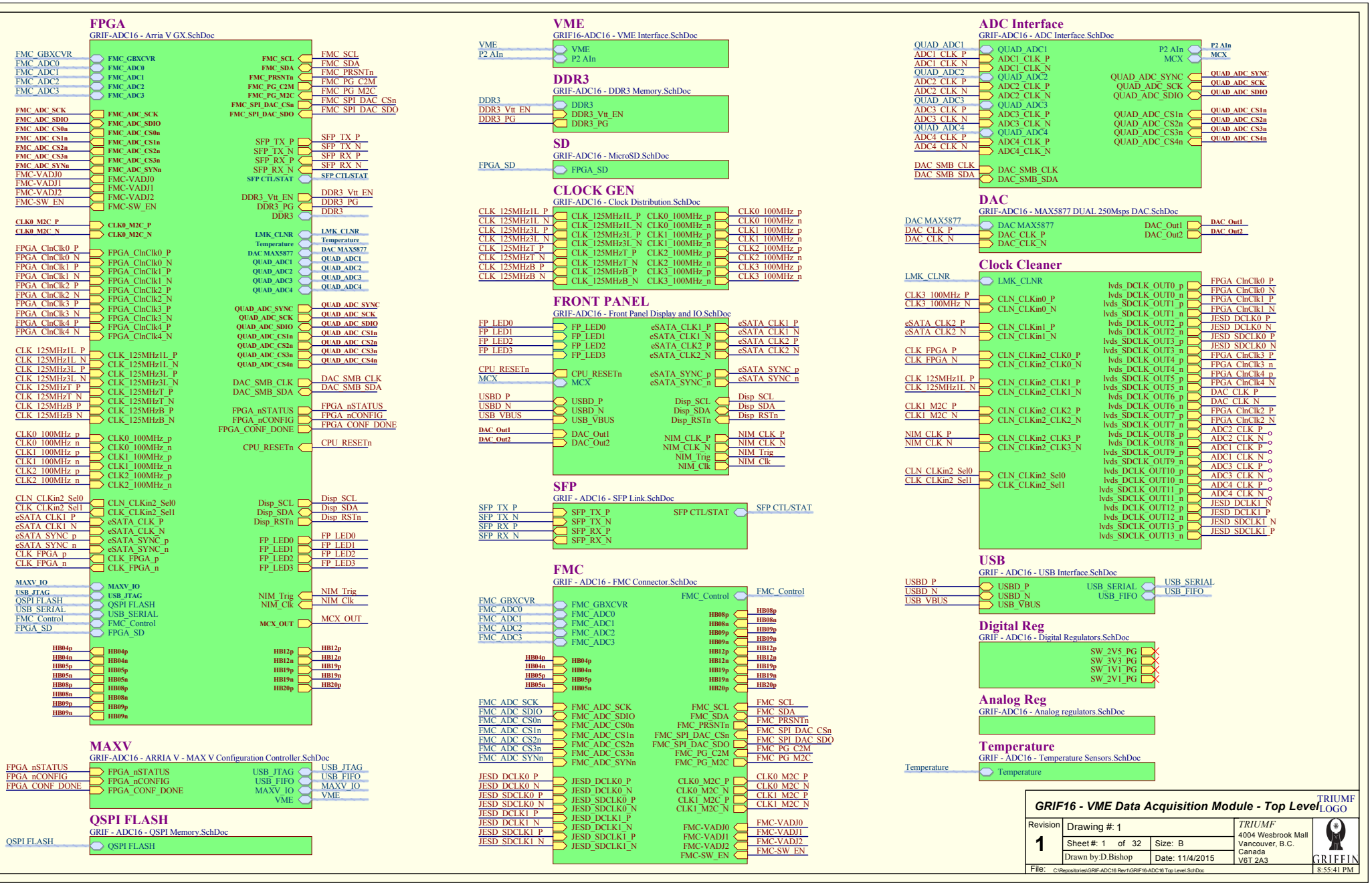
FPGA
GRIF-ADC16 - Arria V GX.SchDoc
FMC_GBXCVR
FMC_ADC0
FMC_ADC1
FMC_ADC2
FMC_ADC3
FMC_ADC_SCK
FMC_ADC_SDIO
FMC_ADC_CS0n
FMC_ADC_CS1n
FMC_ADC_CS2n
FMC_ADC_CS3n
FMC_ADC_SYNn
FMC-VADJ0
FMC-VADJ1
FMC-VADJ2
FMC-SW_EN
CLK0_M2C_P
CLK0_M2C_N
FPGA_ClnClk0_P
FPGA_ClnClk0_N
FPGA_ClnClk1_P
FPGA_ClnClk1_N
FPGA_ClnClk2_P
FPGA_ClnClk2_N
FPGA_ClnClk3_P
FPGA_ClnClk3_N
FPGA_ClnClk4_P
FPGA_ClnClk4_N
CLK_125MHz1L_P
CLK_125MHz1L_N
CLK_125MHz3L_P
CLK_125MHz3L_N
CLK_125MHzT_P
CLK_125MHzT_N
CLK_125MHzB_P
CLK_125MHzB_N
CLK0_100MHz_p
CLK0_100MHz_n
CLK1_100MHz_p
CLK1_100MHz_n
CLK2_100MHz_p
CLK2_100MHz_n
CLN_CLKin2_Sel0
CLK_CLKin2_Sel1
eSATA_CLK1_P
eSATA_CLK1_N
eSATA_SYNC_p
eSATA_SYNC_n
CLK_FPGA_p
CLK_FPGA_n
MAXV_IO
USB_JTAG
QSPI FLASH
USB_SERIAL
FMC_Control
FPGA_SD
HB04p
HB04n
HB05p
HB05n
HB08p
HB08n
HB09p
HB09n
FMC_SCL
FMC_SDA
FMC_PRSNTn
FMC_PG_C2M
FMC_PG_M2C
FMC_SPI_DAC_CSn
FMC_SPI_DAC_SDO
SFP_TX_P
SFP_TX_N
SFP_RX_P
SFP_RX_N
SFP CTL/STAT
DDR3_Vtt_EN
DDR3_PG
DDR3
LMK_CLNR
Temperature
DAC MAX5877
QUAD_ADC1
QUAD_ADC2
QUAD_ADC3
QUAD_ADC4
QUAD_ADC_SYNC
QUAD_ADC_SCK
QUAD_ADC_SDIO
QUAD_ADC_CS1n
QUAD_ADC_CS2n
QUAD_ADC_CS3n
QUAD_ADC_CS4n
DAC_SMB_CLK
DAC_SMB_SDA
FPGA_nSTATUS
FPGA_nCONFIG
FPGA_CONF_DONE
CPU_RESETn
Disp_SCL
Disp_SDA
Disp_RSTn
FP_LED0
FP_LED1
FP_LED2
FP_LED3
NIM_Trig
NIM_Clk
MCX_OUT
HB12p
HB12n
HB19p
HB19n
HB20p
VME
GRIF16-ADC16 - VME Interface.SchDoc
P2 AIn
DDR3
GRIF-ADC16 - DDR3 Memory.SchDoc
SD
GRIF-ADC16 - MicroSD.SchDoc
CLOCK GEN
GRIF-ADC16 - Clock Distribution.SchDoc
CLK0_100MHz_p
CLK0_100MHz_n
CLK1_100MHz_p
CLK1_100MHz_n
CLK2_100MHz_p
CLK2_100MHz_n
CLK3_100MHz_p
CLK3_100MHz_n
FRONT PANEL
GRIF-ADC16 - Front Panel Display and IO.SchDoc
eSATA_CLK1_P
eSATA_CLK1_N
eSATA_CLK2_P
eSATA_CLK2_N
eSATA_SYNC_p
eSATA_SYNC_n
USBD_P
USBD_N
USB_VBUS
NIM_CLK_P
NIM_CLK_N
NIM_Trig
NIM_Clk
SFP
GRIF - ADC16 - SFP Link.SchDoc
FMC
GRIF - ADC16 - FMC Connector.SchDoc
HB08p
HB08n
HB09p
HB09n
HB12p
HB12n
HB19p
HB19n
HB20p
JESD_DCLK0_P
JESD_DCLK0_N
JESD_SDCLK0_P
JESD_SDCLK0_N
JESD_DCLK1_P
JESD_DCLK1_N
JESD_SDCLK1_P
JESD_SDCLK1_N
CLK0_M2C_P
CLK0_M2C_N
CLK1_M2C_P
CLK1_M2C_N
FMC-VADJ0
FMC-VADJ1
FMC-VADJ2
FMC-SW_EN
ADC Interface
GRIF-ADC16 - ADC Interface.SchDoc
QUAD_ADC1
ADC1_CLK_P
ADC1_CLK_N
QUAD_ADC2
ADC2_CLK_P
ADC2_CLK_N
QUAD_ADC3
ADC3_CLK_P
ADC3_CLK_N
QUAD_ADC4
ADC4_CLK_P
ADC4_CLK_N
DAC_SMB_CLK
DAC_SMB_SDA
P2 AIn
MCX
QUAD_ADC_SYNC
QUAD_ADC_SCK
QUAD_ADC_SDIO
QUAD_ADC_CS1n
QUAD_ADC_CS2n
QUAD_ADC_CS3n
QUAD_ADC_CS4n
DAC
GRIF-ADC16 - MAX5877 DUAL 250Msps DAC.SchDoc
DAC MAX5877
DAC_CLK_P
DAC_CLK_N
DAC_Out1
DAC_Out2
Clock Cleaner
LMK_CLNR
CLK3_100MHz_P
CLK3_100MHz_N
eSATA_CLK2_P
eSATA_CLK2_N
CLK_FPGA_P
CLK_FPGA_N
CLK_125MHz1L_P
CLK_125MHz1L_N
CLK1_M2C_P
CLK1_M2C_N
NIM_CLK_P
NIM_CLK_N
CLN_CLKin2_Sel0
CLK_CLKin2_Sel1
CLN_CLKin0_P
CLN_CLKin0_N
CLN_CLKin1_P
CLN_CLKin1_N
CLN_CLKin2_CLK0_P
CLN_CLKin2_CLK0_N
CLN_CLKin2_CLK1_P
CLN_CLKin2_CLK1_N
CLN_CLKin2_CLK2_P
CLN_CLKin2_CLK2_N
CLN_CLKin2_CLK3_P
CLN_CLKin2_CLK3_N
CLN_CLKin2_Sel0
CLK_CLKin2_Sel1
lvds_DCLK_OUT0_p
lvds_DCLK_OUT0_n
lvds_SDCLK_OUT1_p
lvds_SDCLK_OUT1_n
lvds_DCLK_OUT2_p
lvds_DCLK_OUT2_n
lvds_SDCLK_OUT3_p
lvds_SDCLK_OUT3_n
lvds_DCLK_OUT4_p
lvds_DCLK_OUT4_n
lvds_SDCLK_OUT5_p
lvds_SDCLK_OUT5_n
lvds_DCLK_OUT6_p
lvds_DCLK_OUT6_n
lvds_DCLK_OUT7_p
lvds_DCLK_OUT7_n
lvds_DCLK_OUT8_p
lvds_DCLK_OUT8_n
lvds_SDCLK_OUT9_p
lvds_SDCLK_OUT9_n
lvds_DCLK_OUT10_p
lvds_DCLK_OUT10_n
lvds_SDCLK_OUT11_p
lvds_SDCLK_OUT11_n
lvds_DCLK_OUT12_p
lvds_DCLK_OUT12_n
lvds_SDCLK_OUT13_p
lvds_SDCLK_OUT13_n
USB
GRIF - ADC16 - USB Interface.SchDoc
Digital Reg
GRIF - ADC16 - Digital Regulators.SchDoc
SW_2V5_PG
SW_3V3_PG
SW_1V1_PG
SW_2V1_PG
Analog Reg
GRIF-ADC16 - Analog regulators.SchDoc
Temperature
GRIF - ADC16 - Temperature Sensors.SchDoc
MAXV
GRIF-ADC16 - ARRIA V - MAX V Configuration Controller.SchDoc
QSPI FLASH
GRIF - ADC16 - QSPI Memory.SchDoc
GRIF16 - VME Data Acquisition Module - Top Level
TRIUMF LOGO
Revision
1
Drawing #: 1
Sheet #: 1 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF16-ADC16 Top Level.SchDoc
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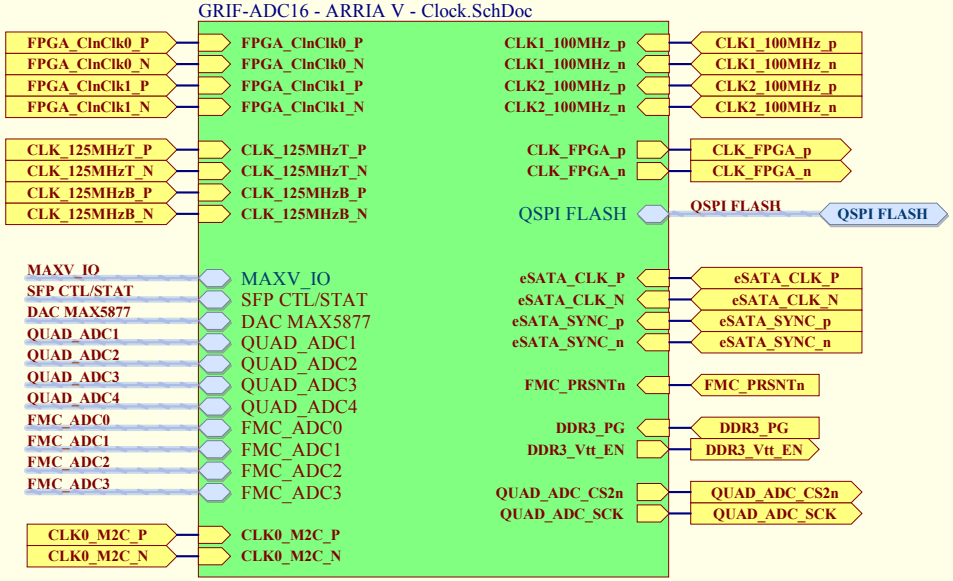
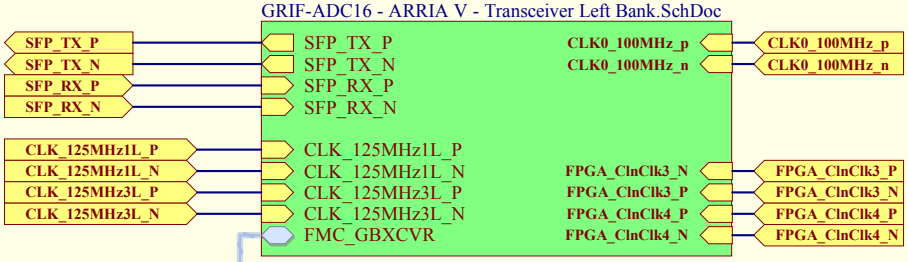
FPGA_CLOCKS

GRIF-ADC16 - ARRIA V - Clock.SchDoc



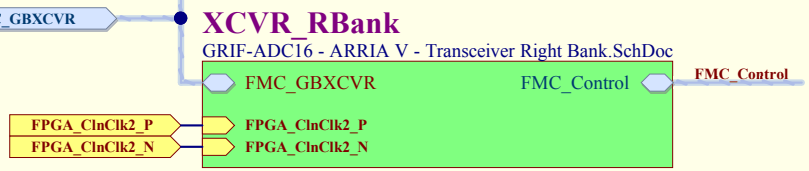
XCVR_LBank

GRIF-ADC16 - ARRIA V - Transceiver Left Bank.SchDoc



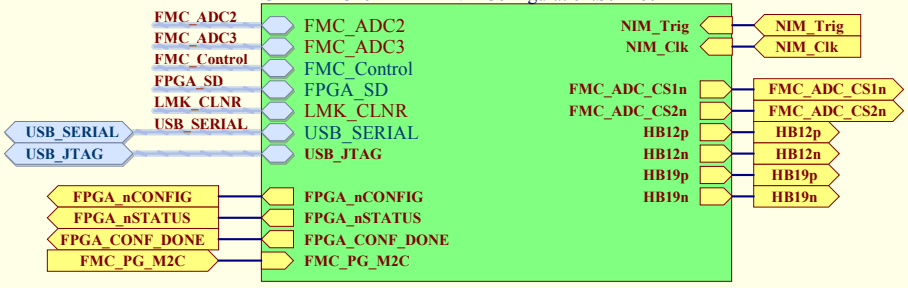
XCVR_RBank

GRIF-ADC16 - ARRIA V - Transceiver Right Bank.SchDoc



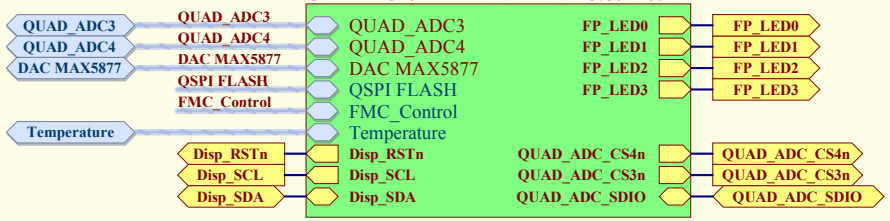
FPGA_CONFIG

GRIF-ADC16 - ARRIA V - Configuration.SchDoc



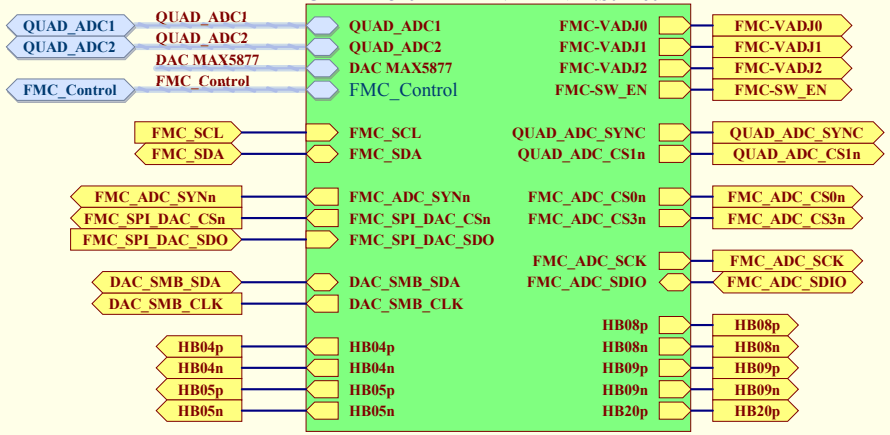
FPGA Bank3

GRIF-ADC16 - ARRIA V - BANK 3.SchDoc



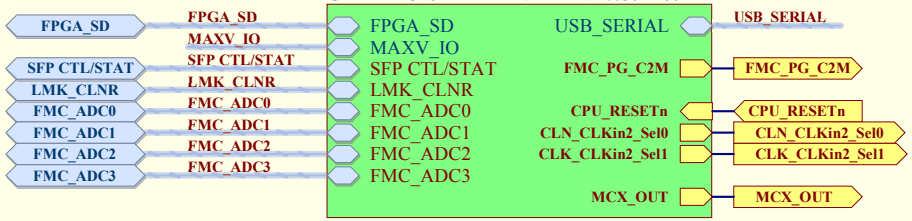
FPGA Bank4

GRIF-ADC16 - ARRIA V - BANK4.SchDoc



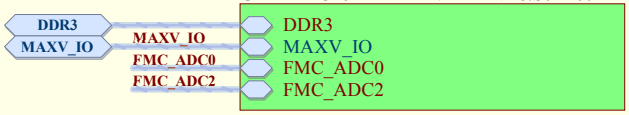
FPGA Bank7

GRIF-ADC16 - ARRIA V - BANK7.SchDoc



FPGA Bank8

GRIF-ADC16 - ARRIA V - BANK8.SchDoc



FPGA_PWR

FPGA_GND

VME - GRIF16 - ARRIA V GX - FPGA

Revision	Drawing #: 2		TRIUMF
1	Sheet #: 2 of 32	Size: A	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: *	Date: 11/4/2015	

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GRIFFIN

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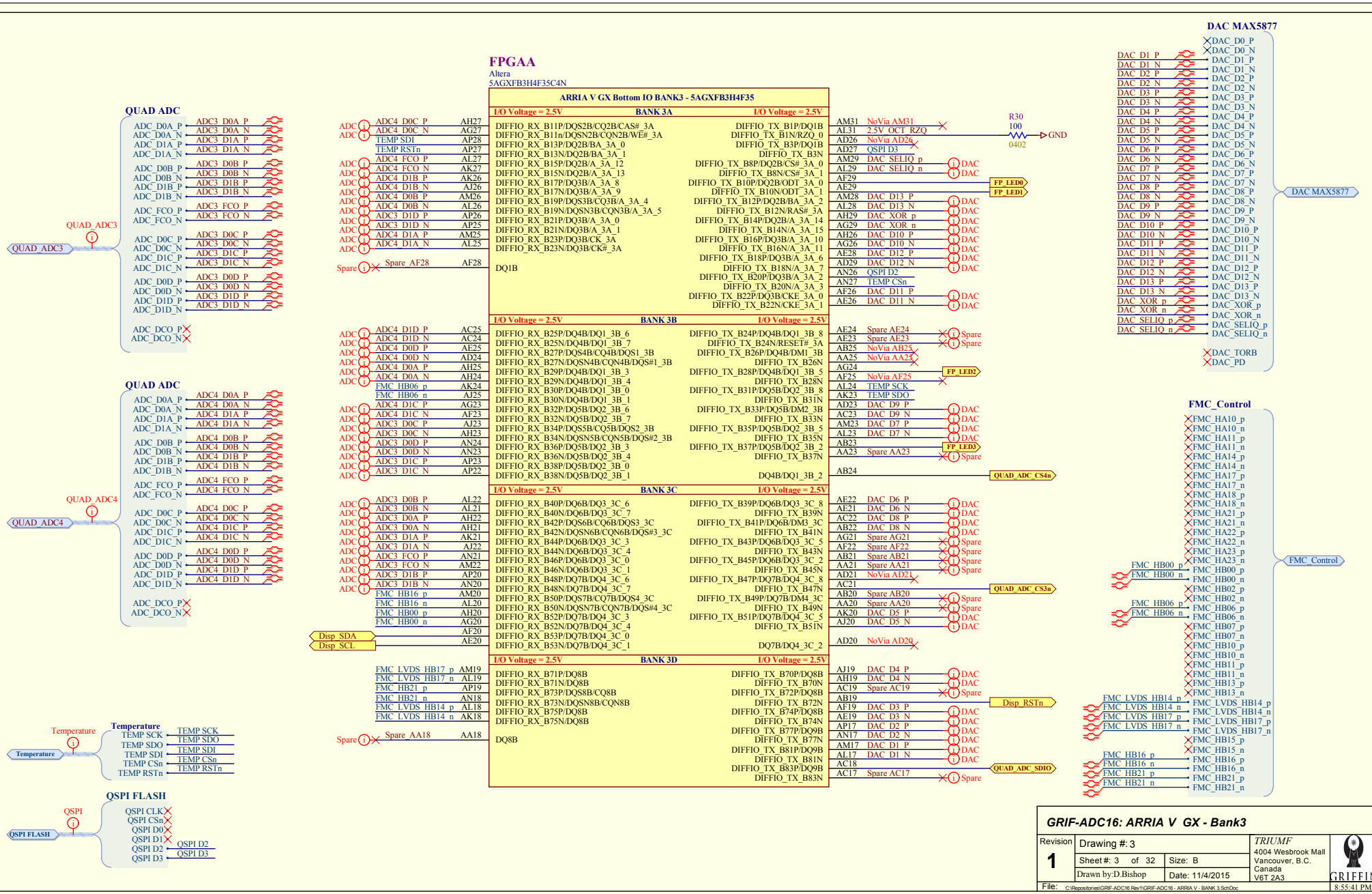
FPGAA
Altera
5AGXFB3H4F35C4N
ARRIA V GX Bottom IO BANK3 - 5AGXFB3H4F35
BANK 3A
BANK 3B
BANK 3C
BANK 3D
I/O Voltage = 2.5V
QUAD ADC
QUAD_ADC3
QUAD_ADC4
Temperature
TEMP SCK
TEMP SDO
TEMP SDI
TEMP CSn
TEMP RSTn
QSPI FLASH
QSPI CLK
QSPI CSn
QSPI D0
QSPI D1
QSPI D2
QSPI D3
DAC MAX5877
FMC_Control
GRIF-ADC16: ARRIA V GX - Bank3
Revision
1
Drawing #: 3
Sheet #: 3 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - BANK 3.SchDoc
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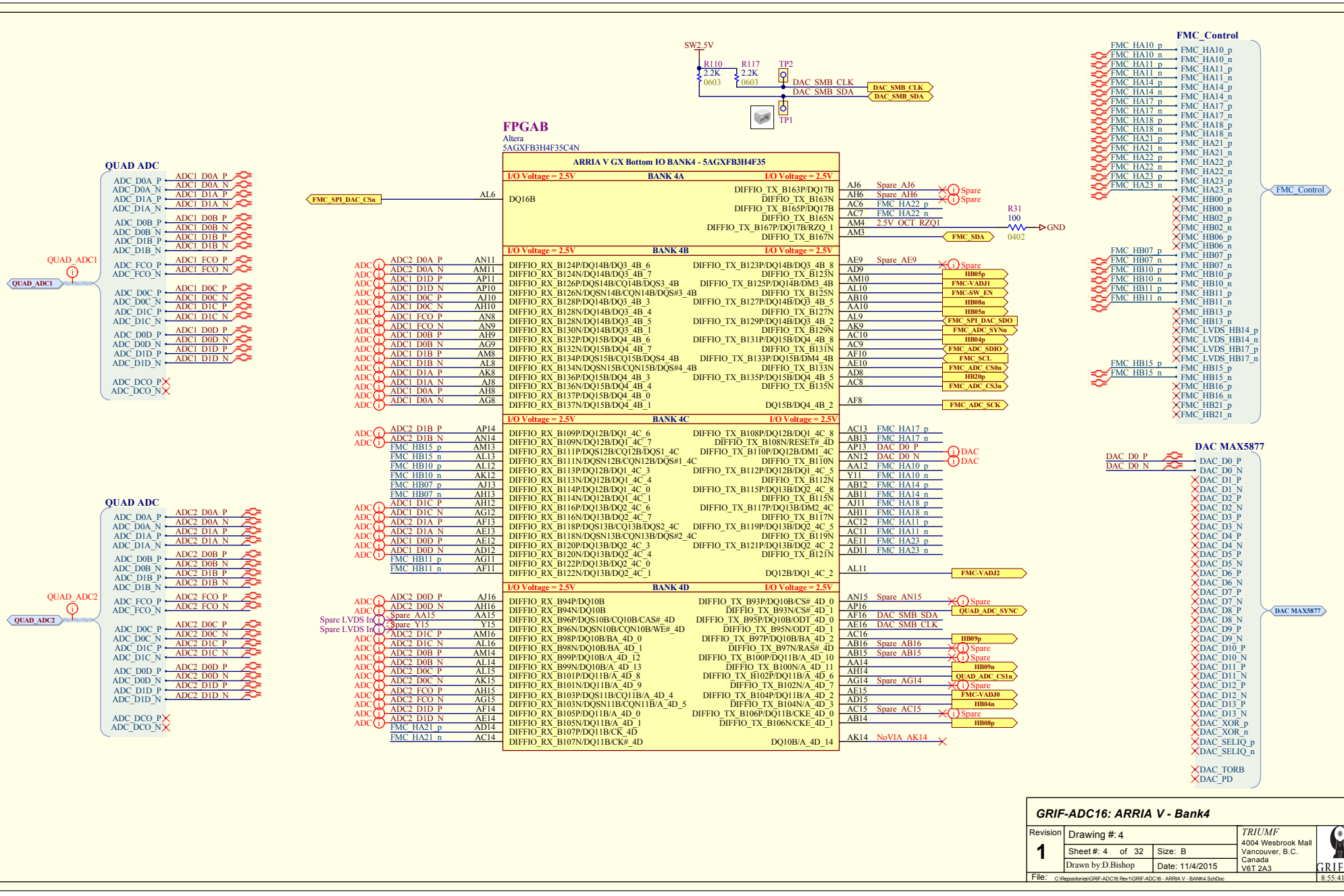
FPGAB
Altera
5AGXFB3H4F35C4N
ARRIA V GX Bottom IO BANK4 - 5AGXFB3H4F35
BANK 4A
BANK 4B
BANK 4C
BANK 4D
I/O Voltage = 2.5V
QUAD ADC
QUAD_ADC1
QUAD_ADC2
FMC_Control
DAC MAX5877
SW2.5V
R110 2.2K 0603
R117 2.2K 0603
TP2
TP1
DAC_SMB_CLK
DAC_SMB_SDA
R31 100 0402
GND
FMC_SPI_DAC_CSn
FMC_SDA
FMC-VADJ1
FMC-SW_EN
FMC-VADJ2
FMC-VADJ0
QUAD_ADC_SYNC
QUAD_ADC_CS1n
GRIF-ADC16: ARRIA V - Bank4
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
Revision 1
Drawing #: 4
Sheet #: 4 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
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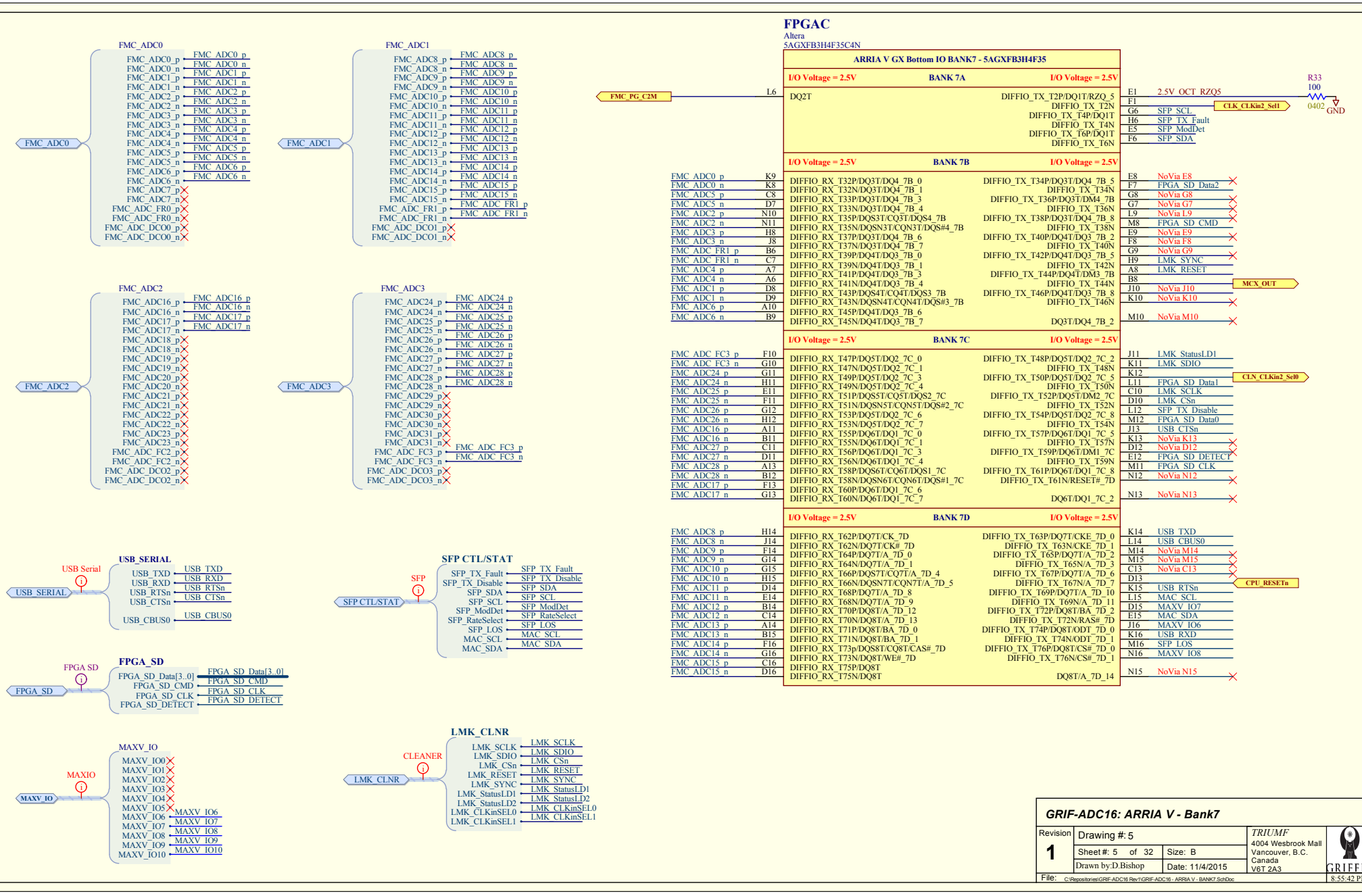
FMC_ADC0
FMC_ADC0_p
FMC_ADC0_n
FMC_ADC1_p
FMC_ADC1_n
FMC_ADC2_p
FMC_ADC2_n
FMC_ADC3_p
FMC_ADC3_n
FMC_ADC4_p
FMC_ADC4_n
FMC_ADC5_p
FMC_ADC5_n
FMC_ADC6_p
FMC_ADC6_n
FMC_ADC7_p
FMC_ADC7_n
FMC_ADC_FR0_p
FMC_ADC_FR0_n
FMC_ADC_DCO0_p
FMC_ADC_DCO0_n
FMC_ADC1
FMC_ADC8_p
FMC_ADC8_n
FMC_ADC9_p
FMC_ADC9_n
FMC_ADC10_p
FMC_ADC10_n
FMC_ADC11_p
FMC_ADC11_n
FMC_ADC12_p
FMC_ADC12_n
FMC_ADC13_p
FMC_ADC13_n
FMC_ADC14_p
FMC_ADC14_n
FMC_ADC15_p
FMC_ADC15_n
FMC_ADC_FR1_p
FMC_ADC_FR1_n
FMC_ADC_DCO1_p
FMC_ADC_DCO1_n
FMC_ADC2
FMC_ADC16_p
FMC_ADC16_n
FMC_ADC17_p
FMC_ADC17_n
FMC_ADC18_p
FMC_ADC18_n
FMC_ADC19_p
FMC_ADC19_n
FMC_ADC20_p
FMC_ADC20_n
FMC_ADC21_p
FMC_ADC21_n
FMC_ADC22_p
FMC_ADC22_n
FMC_ADC23_p
FMC_ADC23_n
FMC_ADC_FC2_p
FMC_ADC_FC2_n
FMC_ADC_DCO2_p
FMC_ADC_DCO2_n
FMC_ADC3
FMC_ADC24_p
FMC_ADC24_n
FMC_ADC25_p
FMC_ADC25_n
FMC_ADC26_p
FMC_ADC26_n
FMC_ADC27_p
FMC_ADC27_n
FMC_ADC28_p
FMC_ADC28_n
FMC_ADC29_p
FMC_ADC29_n
FMC_ADC30_p
FMC_ADC30_n
FMC_ADC31_p
FMC_ADC31_n
FMC_ADC_FC3_p
FMC_ADC_FC3_n
FMC_ADC_DCO3_p
FMC_ADC_DCO3_n
USB_SERIAL
USB Serial
USB_TXD
USB_RXD
USB_RTSn
USB_CTSn
USB_CBUS0
SFP CTL/STAT
SFP
SFP_TX_Fault
SFP_TX_Disable
SFP_SDA
SFP_SCL
SFP_ModDet
SFP_RateSelect
SFP_LOS
MAC_SCL
MAC_SDA
FPGA_SD
FPGA SD
FPGA_SD_Data[3..0]
FPGA_SD_CMD
FPGA_SD_CLK
FPGA_SD_DETECT
MAXV_IO
MAXIO
MAXV_IO0
MAXV_IO1
MAXV_IO2
MAXV_IO3
MAXV_IO4
MAXV_IO5
MAXV_IO6
MAXV_IO7
MAXV_IO8
MAXV_IO9
MAXV_IO10
LMK_CLNR
CLEANER
LMK_SCLK
LMK_SDIO
LMK_CSn
LMK_RESET
LMK_SYNC
LMK_StatusLD1
LMK_StatusLD2
LMK_CLKinSEL0
LMK_CLKinSEL1
FPGAC
Altera
5AGXFB3H4F35C4N
ARRIA V GX Bottom IO BANK7 - 5AGXFB3H4F35
I/O Voltage = 2.5V
BANK 7A
I/O Voltage = 2.5V
FMC_PG_C2M
L6
DQ2T
DIFFIO_TX_T2P/DQ1T/RZQ_5
DIFFIO_TX_T2N
DIFFIO_TX_T4P/DQ1T
DIFFIO_TX_T4N
DIFFIO_TX_T6P/DQ1T
DIFFIO_TX_T6N
E1 2.5V_OCT_RZQ5
F1
G6 SFP_SCL
H6 SFP_TX_Fault
E5 SFP_ModDet
F6 SFP_SDA
R33
100
0402
GND
CLK_CLKin2_Sel1
I/O Voltage = 2.5V
BANK 7B
I/O Voltage = 2.5V
FMC_ADC0_p K9
FMC_ADC0_n K8
FMC_ADC5_p C8
FMC_ADC5_n D7
FMC_ADC2_p N10
FMC_ADC2_n N11
FMC_ADC3_p H8
FMC_ADC3_n J8
FMC_ADC_FR1_p B6
FMC_ADC_FR1_n C7
FMC_ADC4_p A7
FMC_ADC4_n A6
FMC_ADC1_p D8
FMC_ADC1_n D9
FMC_ADC6_p A10
FMC_ADC6_n B9
DIFFIO_RX_T32P/DQ3T/DQ4_7B_0
DIFFIO_RX_T32N/DQ3T/DQ4_7B_1
DIFFIO_RX_T33P/DQ3T/DQ4_7B_3
DIFFIO_RX_T33N/DQ3T/DQ4_7B_4
DIFFIO_RX_T35P/DQS3T/CQ3T/DQS4_7B
DIFFIO_RX_T35N/DQSN3T/CQN3T/DQS#4_7B
DIFFIO_RX_T37P/DQ3T/DQ4_7B_6
DIFFIO_RX_T37N/DQ3T/DQ4_7B_7
DIFFIO_RX_T39P/DQ4T/DQ3_7B_0
DIFFIO_RX_T39N/DQ4T/DQ3_7B_1
DIFFIO_RX_T41P/DQ4T/DQ3_7B_3
DIFFIO_RX_T41N/DQ4T/DQ3_7B_4
DIFFIO_RX_T43P/DQS4T/CQ4T/DQS3_7B
DIFFIO_RX_T43N/DQSN4T/CQN4T/DQS#3_7B
DIFFIO_RX_T45P/DQ4T/DQ3_7B_6
DIFFIO_RX_T45N/DQ4T/DQ3_7B_7
DIFFIO_TX_T34P/DQ3T/DQ4_7B_5
DIFFIO_TX_T34N
DIFFIO_TX_T36P/DQ3T/DM4_7B
DIFFIO_TX_T36N
DIFFIO_TX_T38P/DQ3T/DQ4_7B_8
DIFFIO_TX_T38N
DIFFIO_TX_T40P/DQ4T/DQ3_7B_2
DIFFIO_TX_T40N
DIFFIO_TX_T42P/DQ4T/DQ3_7B_5
DIFFIO_TX_T42N
DIFFIO_TX_T44P/DQ4T/DM3_7B
DIFFIO_TX_T44N
DIFFIO_TX_T46P/DQ4T/DQ3_7B_8
DIFFIO_TX_T46N
DQ3T/DQ4_7B_2
E8 NoVia E8
F7 FPGA_SD_Data2
G8 NoVia G8
G7 NoVia G7
L9 NoVia L9
M8 FPGA_SD_CMD
E9 NoVia E9
F8 NoVia F8
G9 NoVia G9
H9 LMK_SYNC
A8 LMK_RESET
B8
J10 NoVia J10
K10 NoVia K10
M10 NoVia M10
MCX_OUT
I/O Voltage = 2.5V
BANK 7C
I/O Voltage = 2.5V
FMC_ADC_FC3_p F10
FMC_ADC_FC3_n G10
FMC_ADC24_p G11
FMC_ADC24_n H11
FMC_ADC25_p E11
FMC_ADC25_n F11
FMC_ADC26_p G12
FMC_ADC26_n H12
FMC_ADC16_p A11
FMC_ADC16_n B11
FMC_ADC27_p C11
FMC_ADC27_n D11
FMC_ADC28_p A13
FMC_ADC28_n B12
FMC_ADC17_p F13
FMC_ADC17_n G13
DIFFIO_RX_T47P/DQ5T/DQ2_7C_0
DIFFIO_RX_T47N/DQ5T/DQ2_7C_1
DIFFIO_RX_T49P/DQ5T/DQ2_7C_3
DIFFIO_RX_T49N/DQ5T/DQ2_7C_4
DIFFIO_RX_T51P/DQS5T/CQ5T/DQS2_7C
DIFFIO_RX_T51N/DQSN5T/CQN5T/DQS#2_7C
DIFFIO_RX_T53P/DQ5T/DQ2_7C_6
DIFFIO_RX_T53N/DQ5T/DQ2_7C_7
DIFFIO_RX_T55P/DQ6T/DQ1_7C_0
DIFFIO_RX_T55N/DQ6T/DQ1_7C_1
DIFFIO_RX_T56P/DQ6T/DQ1_7C_3
DIFFIO_RX_T56N/DQ6T/DQ1_7C_4
DIFFIO_RX_T58P/DQS6T/CQ6T/DQS1_7C
DIFFIO_RX_T58N/DQSN6T/CQN6T/DQS#1_7C
DIFFIO_RX_T60P/DQ6T/DQ1_7C_6
DIFFIO_RX_T60N/DQ6T/DQ1_7C_7
DIFFIO_TX_T48P/DQ5T/DQ2_7C_2
DIFFIO_TX_T48N
DIFFIO_TX_T50P/DQ5T/DQ2_7C_5
DIFFIO_TX_T50N
DIFFIO_TX_T52P/DQ5T/DM2_7C
DIFFIO_TX_T52N
DIFFIO_TX_T54P/DQ5T/DQ2_7C_8
DIFFIO_TX_T54N
DIFFIO_TX_T57P/DQ6T/DQ1_7C_5
DIFFIO_TX_T57N
DIFFIO_TX_T59P/DQ6T/DM1_7C
DIFFIO_TX_T59N
DIFFIO_TX_T61P/DQ6T/DQ1_7C_8
DIFFIO_TX_T61N/RESET#_7D
DQ6T/DQ1_7C_2
J11 LMK_StatusLD1
K11 LMK_SDIO
K12
L11 FPGA_SD_Data1
C10 LMK_SCLK
D10 LMK_CSn
L12 SFP_TX_Disable
M12 FPGA_SD_Data0
J13 USB_CTSn
K13 NoVia K13
D12 NoVia D12
E12 FPGA_SD_DETECT
M11 FPGA_SD_CLK
N12 NoVia N12
N13 NoVia N13
CLN_CLKin2_Sel0
I/O Voltage = 2.5V
BANK 7D
I/O Voltage = 2.5V
FMC_ADC8_p H14
FMC_ADC8_n J14
FMC_ADC9_p F14
FMC_ADC9_n G14
FMC_ADC10_p G15
FMC_ADC10_n H15
FMC_ADC11_p D14
FMC_ADC11_n E14
FMC_ADC12_p B14
FMC_ADC12_n C14
FMC_ADC13_p A14
FMC_ADC13_n B15
FMC_ADC14_p F16
FMC_ADC14_n G16
FMC_ADC15_p C16
FMC_ADC15_n D16
DIFFIO_RX_T62P/DQ7T/CK_7D
DIFFIO_RX_T62N/DQ7T/CK#_7D
DIFFIO_RX_T64P/DQ7T/A_7D_0
DIFFIO_RX_T64N/DQ7T/A_7D_1
DIFFIO_RX_T66P/DQS7T/CQ7T/A_7D_4
DIFFIO_RX_T66N/DQSN7T/CQN7T/A_7D_5
DIFFIO_RX_T68P/DQ7T/A_7D_8
DIFFIO_RX_T68N/DQ7T/A_7D_9
DIFFIO_RX_T70P/DQ8T/A_7D_12
DIFFIO_RX_T70N/DQ8T/A_7D_13
DIFFIO_RX_T71P/DQ8T/BA_7D_0
DIFFIO_RX_T71N/DQ8T/BA_7D_1
DIFFIO_RX_T73p/DQS8T/CQ8T/CAS#_7D
DIFFIO_RX_T73N/DQ8T/WE#_7D
DIFFIO_RX_T75P/DQ8T
DIFFIO_RX_T75N/DQ8T
DIFFIO_TX_T63P/DQ7T/CKE_7D_0
DIFFIO_TX_T63N/CKE_7D_1
DIFFIO_TX_T65P/DQ7T/A_7D_2
DIFFIO_TX_T65N/A_7D_3
DIFFIO_TX_T67P/DQ7T/A_7D_6
DIFFIO_TX_T67N/A_7D_7
DIFFIO_TX_T69P/DQ7T/A_7D_10
DIFFIO_TX_T69N/A_7D_11
DIFFIO_TX_T72P/DQ8T/BA_7D_2
DIFFIO_TX_T72N/RAS#_7D
DIFFIO_TX_T74P/DQ8T/ODT_7D_0
DIFFIO_TX_T74N/ODT_7D_1
DIFFIO_TX_T76P/DQ8T/CS#_7D_0
DIFFIO_TX_T76N/CS#_7D_1
DQ8T/A_7D_14
K14 USB_TXD
L14 USB_CBUS0
M14 NoVia M14
M15 NoVia M15
C13 NoVia C13
D13
K15 USB_RTSn
L15 MAC_SCL
D15 MAXV_IO7
E15 MAC_SDA
J16 MAXV_IO6
K16 USB_RXD
M16 SFP_LOS
N16 MAXV_IO8
N15 NoVia N15
CPU_RESETn
GRIF-ADC16: ARRIA V - Bank7
Revision
1
Drawing #: 5
Sheet #: 5 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - BANK7.SchDoc
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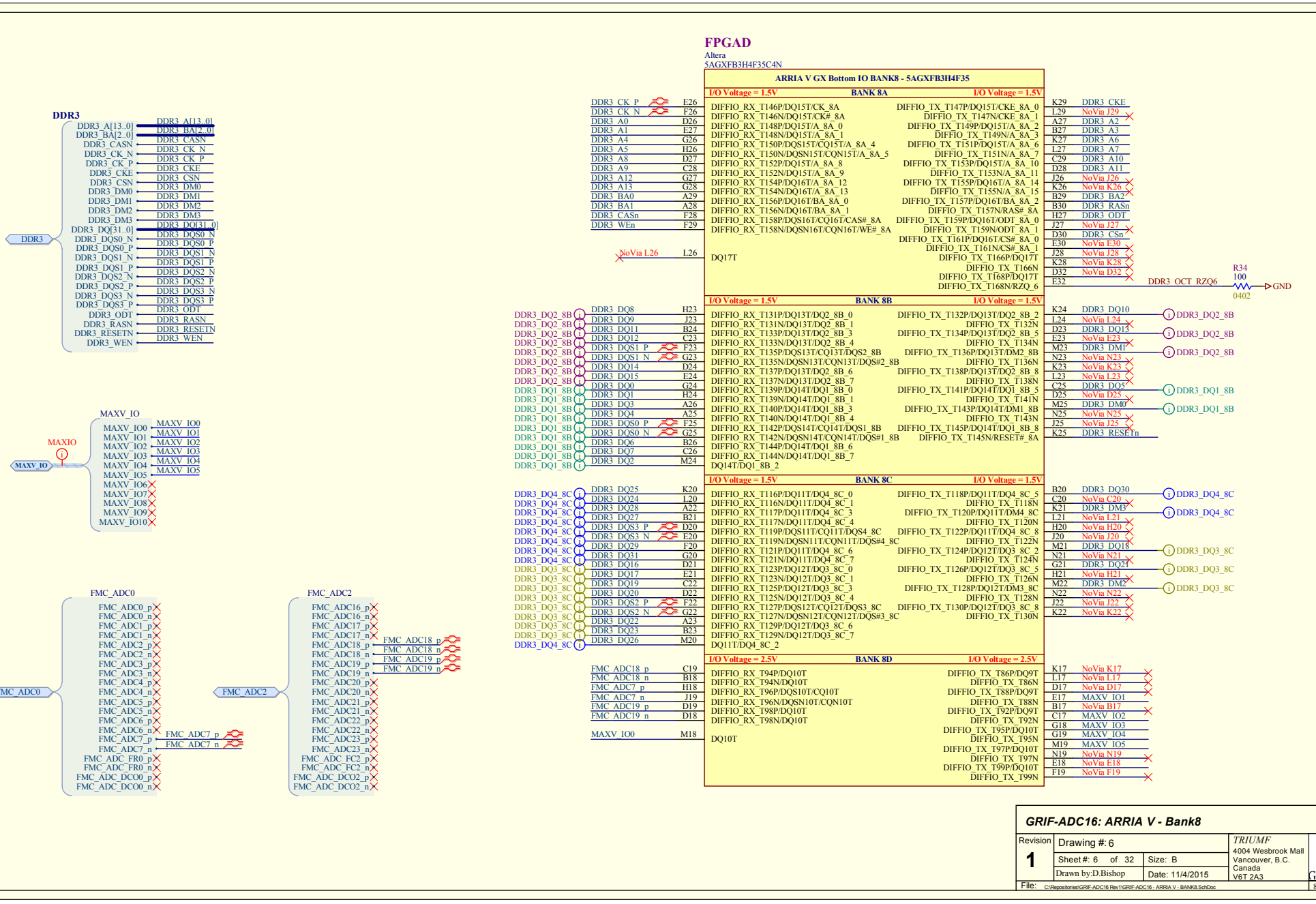
FPGAD
Altera
5AGXFB3H4F35C4N
ARRIA V GX Bottom IO BANK8 - 5AGXFB3H4F35
I/O Voltage = 1.5V
BANK 8A
I/O Voltage = 1.5V
DIFFIO_RX_T146P/DQ15T/CK_8A
DIFFIO_RX_T146N/DQ15T/CK#_8A
DIFFIO_RX_T148P/DQ15T/A_8A_0
DIFFIO_RX_T148N/DQ15T/A_8A_1
DIFFIO_RX_T150P/DQS15T/CQ15T/A_8A_4
DIFFIO_RX_T150N/DQSN15T/CQN15T/A_8A_5
DIFFIO_RX_T152P/DQ15T/A_8A_8
DIFFIO_RX_T152N/DQ15T/A_8A_9
DIFFIO_RX_T154P/DQ16T/A_8A_12
DIFFIO_RX_T154N/DQ16T/A_8A_13
DIFFIO_RX_T156P/DQ16T/BA_8A_0
DIFFIO_RX_T156N/DQ16T/BA_8A_1
DIFFIO_RX_T158P/DQS16T/CQ16T/CAS#_8A
DIFFIO_RX_T158N/DQSN16T/CQN16T/WE#_8A
DQ17T
DIFFIO_TX_T147P/DQ15T/CKE_8A_0
DIFFIO_TX_T147N/CKE_8A_1
DIFFIO_TX_T149P/DQ15T/A_8A_2
DIFFIO_TX_T149N/A_8A_3
DIFFIO_TX_T151P/DQ15T/A_8A_6
DIFFIO_TX_T151N/A_8A_7
DIFFIO_TX_T153P/DQ15T/A_8A_10
DIFFIO_TX_T153N/A_8A_11
DIFFIO_TX_T155P/DQ16T/A_8A_14
DIFFIO_TX_T155N/A_8A_15
DIFFIO_TX_T157P/DQ16T/BA_8A_2
DIFFIO_TX_T157N/RAS#_8A
DIFFIO_TX_T159P/DQ16T/ODT_8A_0
DIFFIO_TX_T159N/ODT_8A_1
DIFFIO_TX_T161P/DQ16T/CS#_8A_0
DIFFIO_TX_T161N/CS#_8A_1
DIFFIO_TX_T166P/DQ17T
DIFFIO_TX_T166N
DIFFIO_TX_T168P/DQ17T
DIFFIO_TX_T168N/RZQ_6
I/O Voltage = 1.5V
BANK 8B
I/O Voltage = 1.5V
DIFFIO_RX_T131P/DQ13T/DQ2_8B_0
DIFFIO_RX_T131N/DQ13T/DQ2_8B_1
DIFFIO_RX_T133P/DQ13T/DQ2_8B_3
DIFFIO_RX_T133N/DQ13T/DQ2_8B_4
DIFFIO_RX_T135P/DQS13T/CQ13T/DQS2_8B
DIFFIO_RX_T135N/DQSN13T/CQN13T/DQS#2_8B
DIFFIO_RX_T137P/DQ13T/DQ2_8B_6
DIFFIO_RX_T137N/DQ13T/DQ2_8B_7
DIFFIO_RX_T139P/DQ14T/DQ1_8B_0
DIFFIO_RX_T139N/DQ14T/DQ1_8B_1
DIFFIO_RX_T140P/DQ14T/DQ1_8B_3
DIFFIO_RX_T140N/DQ14T/DQ1_8B_4
DIFFIO_RX_T142P/DQS14T/CQ14T/DQS1_8B
DIFFIO_RX_T142N/DQSN14T/CQN14T/DQS#1_8B
DIFFIO_RX_T144P/DQ14T/DQ1_8B_6
DIFFIO_RX_T144N/DQ14T/DQ1_8B_7
DQ14T/DQ1_8B_2
DIFFIO_TX_T132P/DQ13T/DQ2_8B_2
DIFFIO_TX_T132N
DIFFIO_TX_T134P/DQ13T/DQ2_8B_5
DIFFIO_TX_T134N
DIFFIO_TX_T136P/DQ13T/DM2_8B
DIFFIO_TX_T136N
DIFFIO_TX_T138P/DQ13T/DQ2_8B_8
DIFFIO_TX_T138N
DIFFIO_TX_T141P/DQ14T/DQ1_8B_5
DIFFIO_TX_T141N
DIFFIO_TX_T143P/DQ14T/DM1_8B
DIFFIO_TX_T143N
DIFFIO_TX_T145P/DQ14T/DQ1_8B_8
DIFFIO_TX_T145N/RESET#_8A
I/O Voltage = 1.5V
BANK 8C
I/O Voltage = 1.5V
DIFFIO_RX_T116P/DQ11T/DQ4_8C_0
DIFFIO_RX_T116N/DQ11T/DQ4_8C_1
DIFFIO_RX_T117P/DQ11T/DQ4_8C_3
DIFFIO_RX_T117N/DQ11T/DQ4_8C_4
DIFFIO_RX_T119P/DQS11T/CQ11T/DQS4_8C
DIFFIO_RX_T119N/DQSN11T/CQN11T/DQS#4_8C
DIFFIO_RX_T121P/DQ11T/DQ4_8C_6
DIFFIO_RX_T121N/DQ11T/DQ4_8C_7
DIFFIO_RX_T123P/DQ12T/DQ3_8C_0
DIFFIO_RX_T123N/DQ12T/DQ3_8C_1
DIFFIO_RX_T125P/DQ12T/DQ3_8C_3
DIFFIO_RX_T125N/DQ12T/DQ3_8C_4
DIFFIO_RX_T127P/DQS12T/CQ12T/DQS3_8C
DIFFIO_RX_T127N/DQSN12T/CQN12T/DQS#3_8C
DIFFIO_RX_T129P/DQ12T/DQ3_8C_6
DIFFIO_RX_T129N/DQ12T/DQ3_8C_7
DQ11T/DQ4_8C_2
DIFFIO_TX_T118P/DQ11T/DQ4_8C_5
DIFFIO_TX_T118N
DIFFIO_TX_T120P/DQ11T/DM4_8C
DIFFIO_TX_T120N
DIFFIO_TX_T122P/DQ11T/DQ4_8C_8
DIFFIO_TX_T122N
DIFFIO_TX_T124P/DQ12T/DQ3_8C_2
DIFFIO_TX_T124N
DIFFIO_TX_T126P/DQ12T/DQ3_8C_5
DIFFIO_TX_T126N
DIFFIO_TX_T128P/DQ12T/DM3_8C
DIFFIO_TX_T128N
DIFFIO_TX_T130P/DQ12T/DQ3_8C_8
DIFFIO_TX_T130N
I/O Voltage = 2.5V
BANK 8D
I/O Voltage = 2.5V
DIFFIO_RX_T94P/DQ10T
DIFFIO_RX_T94N/DQ10T
DIFFIO_RX_T96P/DQS10T/CQ10T
DIFFIO_RX_T96N/DQSN10T/CQN10T
DIFFIO_RX_T98P/DQ10T
DIFFIO_RX_T98N/DQ10T
DQ10T
DIFFIO_TX_T86P/DQ9T
DIFFIO_TX_T86N
DIFFIO_TX_T88P/DQ9T
DIFFIO_TX_T88N
DIFFIO_TX_T92P/DQ9T
DIFFIO_TX_T92N
DIFFIO_TX_T95P/DQ10T
DIFFIO_TX_T95N
DIFFIO_TX_T97P/DQ10T
DIFFIO_TX_T97N
DIFFIO_TX_T99P/DQ10T
DIFFIO_TX_T99N
DDR3
DDR3_A[13..0]
DDR3_BA[2..0]
DDR3_CASN
DDR3_CK_N
DDR3_CK_P
DDR3_CKE
DDR3_CSN
DDR3_DM0
DDR3_DM1
DDR3_DM2
DDR3_DM3
DDR3_DQ[31..0]
DDR3_DQS0_N
DDR3_DQS0_P
DDR3_DQS1_N
DDR3_DQS1_P
DDR3_DQS2_N
DDR3_DQS2_P
DDR3_DQS3_N
DDR3_DQS3_P
DDR3_ODT
DDR3_RASN
DDR3_RESETN
DDR3_WEN
MAXV_IO
MAXIO
MAXV_IO0
MAXV_IO1
MAXV_IO2
MAXV_IO3
MAXV_IO4
MAXV_IO5
MAXV_IO6
MAXV_IO7
MAXV_IO8
MAXV_IO9
MAXV_IO10
FMC_ADC0
FMC_ADC0_p
FMC_ADC0_n
FMC_ADC1_p
FMC_ADC1_n
FMC_ADC2_p
FMC_ADC2_n
FMC_ADC3_p
FMC_ADC3_n
FMC_ADC4_p
FMC_ADC4_n
FMC_ADC5_p
FMC_ADC5_n
FMC_ADC6_p
FMC_ADC6_n
FMC_ADC7_p
FMC_ADC7_n
FMC_ADC_FR0_p
FMC_ADC_FR0_n
FMC_ADC_DCO0_p
FMC_ADC_DCO0_n
FMC_ADC2
FMC_ADC16_p
FMC_ADC16_n
FMC_ADC17_p
FMC_ADC17_n
FMC_ADC18_p
FMC_ADC18_n
FMC_ADC19_p
FMC_ADC19_n
FMC_ADC20_p
FMC_ADC20_n
FMC_ADC21_p
FMC_ADC21_n
FMC_ADC22_p
FMC_ADC22_n
FMC_ADC23_p
FMC_ADC23_n
FMC_ADC_FC2_p
FMC_ADC_FC2_n
FMC_ADC_DCO2_p
FMC_ADC_DCO2_n
DDR3_CK_P E26
DDR3_CK_N F26
DDR3_A0 D26
DDR3_A1 E27
DDR3_A4 G26
DDR3_A5 H26
DDR3_A8 D27
DDR3_A9 C28
DDR3_A12 G27
DDR3_A13 G28
DDR3_BA0 A29
DDR3_BA1 A28
DDR3_CASn F28
DDR3_WEn F29
NoVia L26 L26
DDR3_DQ2_8B
DDR3_DQ8 H23
DDR3_DQ9 J23
DDR3_DQ11 B24
DDR3_DQ12 C23
DDR3_DQS1_P F23
DDR3_DQS1_N G23
DDR3_DQ14 D24
DDR3_DQ15 E24
DDR3_DQ0 G24
DDR3_DQ1 H24
DDR3_DQ3 A26
DDR3_DQ4 A25
DDR3_DQS0_P F25
DDR3_DQS0_N G25
DDR3_DQ6 B26
DDR3_DQ7 C26
DDR3_DQ2 M24
DDR3_DQ4_8C
DDR3_DQ25 K20
DDR3_DQ24 L20
DDR3_DQ28 A22
DDR3_DQ27 B21
DDR3_DQS3_P D20
DDR3_DQS3_N E20
DDR3_DQ29 F20
DDR3_DQ31 G20
DDR3_DQ16 D21
DDR3_DQ17 E21
DDR3_DQ19 C22
DDR3_DQ20 D22
DDR3_DQS2_P F22
DDR3_DQS2_N G22
DDR3_DQ22 A23
DDR3_DQ23 B23
DDR3_DQ26 M20
FMC_ADC18_p C19
FMC_ADC18_n B18
FMC_ADC7_p H18
FMC_ADC7_n J19
FMC_ADC19_p D19
FMC_ADC19_n D18
MAXV_IO0 M18
DDR3_CKE K29
NoVia J29 L29
DDR3_A2 A27
DDR3_A3 B27
DDR3_A6 K27
DDR3_A7 L27
DDR3_A10 C29
DDR3_A11 D28
NoVia J26 J26
NoVia K26 K26
DDR3_BA2 B29
DDR3_RASn B30
DDR3_ODT H27
NoVia J27 J27
DDR3_CSn D30
NoVia E30 E30
NoVia J28 J28
NoVia K28 K28
NoVia D32 D32
E32
DDR3_OCT_RZQ6
R34
100
0402
GND
DDR3_DQ2_8B
DDR3_DQ10 K24
NoVia L24 L24
DDR3_DQ13 D23
NoVia E23 E23
DDR3_DM1 M23
NoVia N23 N23
NoVia K23 K23
NoVia L23 L23
DDR3_DQ5 C25
NoVia D25 D25
DDR3_DM0 M25
NoVia N25 N25
NoVia J25 J25
DDR3_RESETn K25
DDR3_DQ4_8C
DDR3_DQ30 B20
NoVia C20 C20
DDR3_DM3 K21
NoVia L21 L21
NoVia H20 H20
NoVia J20 J20
DDR3_DQ18 M21
NoVia N21 N21
DDR3_DQ21 G21
NoVia H21 H21
DDR3_DM2 M22
NoVia N22 N22
NoVia J22 J22
NoVia K22 K22
DDR3_DQ3_8C
NoVia K17 K17
NoVia L17 L17
NoVia D17 D17
MAXV_IO1 E17
NoVia B17 B17
MAXV_IO2 C17
MAXV_IO3 G18
MAXV_IO4 G19
MAXV_IO5 M19
NoVia N19 N19
NoVia E18 E18
NoVia F19 F19
GRIF-ADC16: ARRIA V - Bank8
Revision
1
Drawing #: 6
Sheet #: 6 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - BANK8.SchDoc
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FPGAE

Altera

5AGXFB3H4F35C4N

ARRIA V GX Tranceiver Left Bank - 5AGXFB3H4F35

BANK L0

ClassName: GB_RX

SFP_RX_P	C142 10nF	RX_L0_p	AK34	GXB_RX_L0P,GXB_REFCLK_L0P	
SFP_RX_N	C143 10nF	RX_L0_n	AK33	GXB_RX_L0N,GXB_REFCLK_L0N	
		CLK_125MHz3L_p	AH34	GXB_RX_L1P,GXB_REFCLK_L1P	
		CLK_125MHz3L_n	AH33	GXB_RX_L1N,GXB_REFCLK_L1N	
		CLK0_100MHz_p	AF34	GXB_RX_L2P,GXB_REFCLK_L2P	
		CLK0_100MHz_n	AF33	GXB_RX_L2N,GXB_REFCLK_L2N	
DP8_M2C_P	C117 10nF	RX_R8_p	AD34	GXB_RX_L3P,GXB_REFCLK_L3P	
DP8_M2C_N	C118 10nF	RX_R8_n	AD33	GXB_RX_L3N,GXB_REFCLK_L3N	
DP9_M2C_P	C119 10nF	RX_R9_p	AB34	GXB_RX_L4P,GXB_REFCLK_L4P	
DP9_M2C_N	C130 10nF	RX_R9_n	AB33	GXB_RX_L4N,GXB_REFCLK_L4N	
		NoVia RX_L5P	Y34	GXB_RX_L5P,GXB_REFCLK_L5P	
		NoVia RX_L5N	Y33	GXB_RX_L5N,GXB_REFCLK_L5N	
		NoVia AA27	AA27	REFCLK0LP	
		NoVia AA28	AA28	REFCLK0LN	
		NoVia W26	W26	REFCLK1LP	
		NoVia W27	W27	REFCLK1LN	

ClassName: GB_TX

GXB_TX_L0P	AJ32	SFP_TX_P	
GXB_TX_L0N	AJ31	SFP_TX_N	
GXB_TX_L1P	AG32	Spare TX_L1P	
GXB_TX_L1N	AG31	Spare TX_L1N	
GXB_TX_L2P	AE32	Spare TX_L2P	
GXB_TX_L2N	AE31	Spare TX_L2N	
GXB_TX_L3P	AC32	DP8_C2M_P	
GXB_TX_L3N	AC31	DP8_C2M_N	
GXB_TX_L4P	AA32	DP9_C2M_P	
GXB_TX_L4N	AA31	DP9_C2M_N	
GXB_TX_L5P	W32	Spare TX_L5P	
GXB_TX_L5N	W31	Spare TX_L5N	

BANK L1

FPGA_ClnClk3_P	FPGA_ClnClk3_P		V34	GXB_RX_L6P,GXB_REFCLK_L6P	
FPGA_ClnClk3_N	FPGA_ClnClk3_N		V33	GXB_RX_L6N,GXB_REFCLK_L6N	
Spare CLK_In1		Spare RX_L7P	T34	GXB_RX_L7P,GXB_REFCLK_L7P	
Spare CLK_In1		Spare RX_L7N	T33	GXB_RX_L7N,GXB_REFCLK_L7N	
Spare CLK_In1		Spare RX_L8P	P34	GXB_RX_L8P,GXB_REFCLK_L8P	
Spare CLK_In1		Spare RX_L8N	P33	GXB_RX_L8N,GXB_REFCLK_L8N	
Spare CLK_In1		Spare RX_L9P	M34	GXB_RX_L9P,GXB_REFCLK_L9P	
Spare CLK_In1		Spare RX_L9N	M33	GXB_RX_L9N,GXB_REFCLK_L9N	
		NoVIA_GB_RX_L10p	K34	GXB_RX_L10P,GXB_REFCLK_L10P	
		NoVIA_GB_RX_L10n	K33	GXB_RX_L10N,GXB_REFCLK_L10N	
		NoVIA_GB_RX_L11p	H34	GXB_RX_L11P,GXB_REFCLK_L11P	
		NoVIA_GB_RX_L11n	H33	GXB_RX_L11N,GXB_REFCLK_L11N	
FPGA_ClnClk4_P	FPGA_ClnClk4_P		U26	EFCLK2LP	
FPGA_ClnClk4_N	FPGA_ClnClk4_N		U27	REFCLK2LN	
		NoVia REFCLK3Lp	R26	REFCLK3LP	
		NoVia REFCLK3Ln	R27	REFCLK3LN	

GXB_TX_L6P	U32	Spare TX_L6P	
GXB_TX_L6N	U31	Spare TX_L6N	
GXB_TX_L7P	R32	Spare TX_L7P	
GXB_TX_L7N	R31	Spare TX_L7N	
GXB_TX_L8P	N32	Spare TX_L8P	
GXB_TX_L8N	N31	Spare TX_L8N	
GXB_TX_L9P	L32	Spare TX_L9P	
GXB_TX_L9N	L31	Spare TX_L9N	
GXB_TX_L10P	J32	Spare TX_L10P	
GXB_TX_L10N	J31	Spare TX_L10N	
GXB_TX_L11P	G32	Spare TX_L11P	
GXB_TX_L11N	G31	Spare TX_L11N	

Reference Resistor

F34	RREF_TL	

Rref1
2K
0402

GND

FMC_GBXCVR

	DP0_C2M_P	
	DP0_C2M_N	
	DP1_C2M_P	
	DP1_C2M_N	
	DP2_C2M_P	
	DP2_C2M_N	
	DP3_C2M_P	
	DP3_C2M_N	
	DP4_C2M_P	
	DP4_C2M_N	
	DP5_C2M_P	
	DP5_C2M_N	
	DP6_C2M_P	
	DP6_C2M_N	
	DP7_C2M_P	
	DP7_C2M_N	
DP8_C2M_P	DP8_C2M_P	
DP8_C2M_N	DP8_C2M_N	
DP9_C2M_P	DP9_C2M_P	
DP9_C2M_N	DP9_C2M_N	
	DP0_M2C_P	
	DP0_M2C_N	
	DP1_M2C_P	
	DP1_M2C_N	
	DP2_M2C_P	
	DP2_M2C_N	
	DP3_M2C_P	
	DP3_M2C_N	
	DP4_M2C_P	
	DP4_M2C_N	
	DP5_M2C_P	
	DP5_M2C_N	
	DP6_M2C_P	
	DP6_M2C_N	
	DP7_M2C_P	
	DP7_M2C_N	
DP8_M2C_P	DP8_M2C_P	
DP8_M2C_N	DP8_M2C_N	
DP9_M2C_P	DP9_M2C_P	
DP9_M2C_N	DP9_M2C_N	
	GBTCLK0_M2C_P	
	GBTCLK0_M2C_N	
	GBTCLK1_M2C_P	
	GBTCLK1_M2C_N	

FMC_GBXCVR

CLK0_100MHz_p → CLK0_100MHz_p
CLK0_100MHz_n → CLK0_100MHz_n

CLK_125MHz3L_p → CLK_125MHz3L_P
CLK_125MHz3L_n → CLK_125MHz3L_N

CLK_125MHz1L_p → CLK_125MHz1L_p
CLK_125MHz1L_n → CLK_125MHz1L_n

SFP_TX_P → SFP_TX_P
SFP_TX_N → SFP_TX_N
SFP_RX_P → SFP_RX_P
SFP_RX_N → SFP_RX_N

GRIF-ADC16: ARRIA V - Transceiver Left Bank

Revision 1	Drawing #: 7		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 7 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - Transceiver Left Bank.SchDoc

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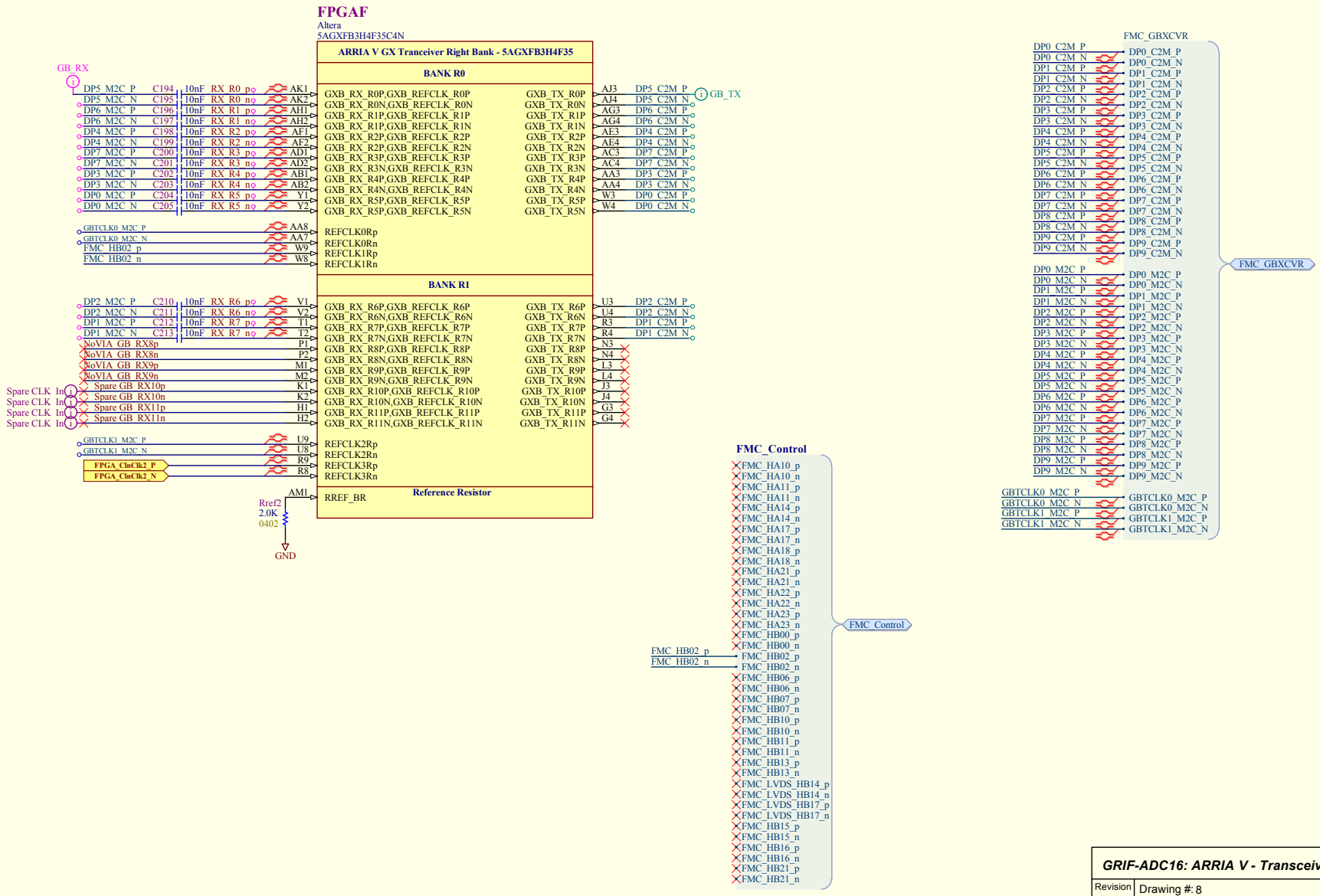
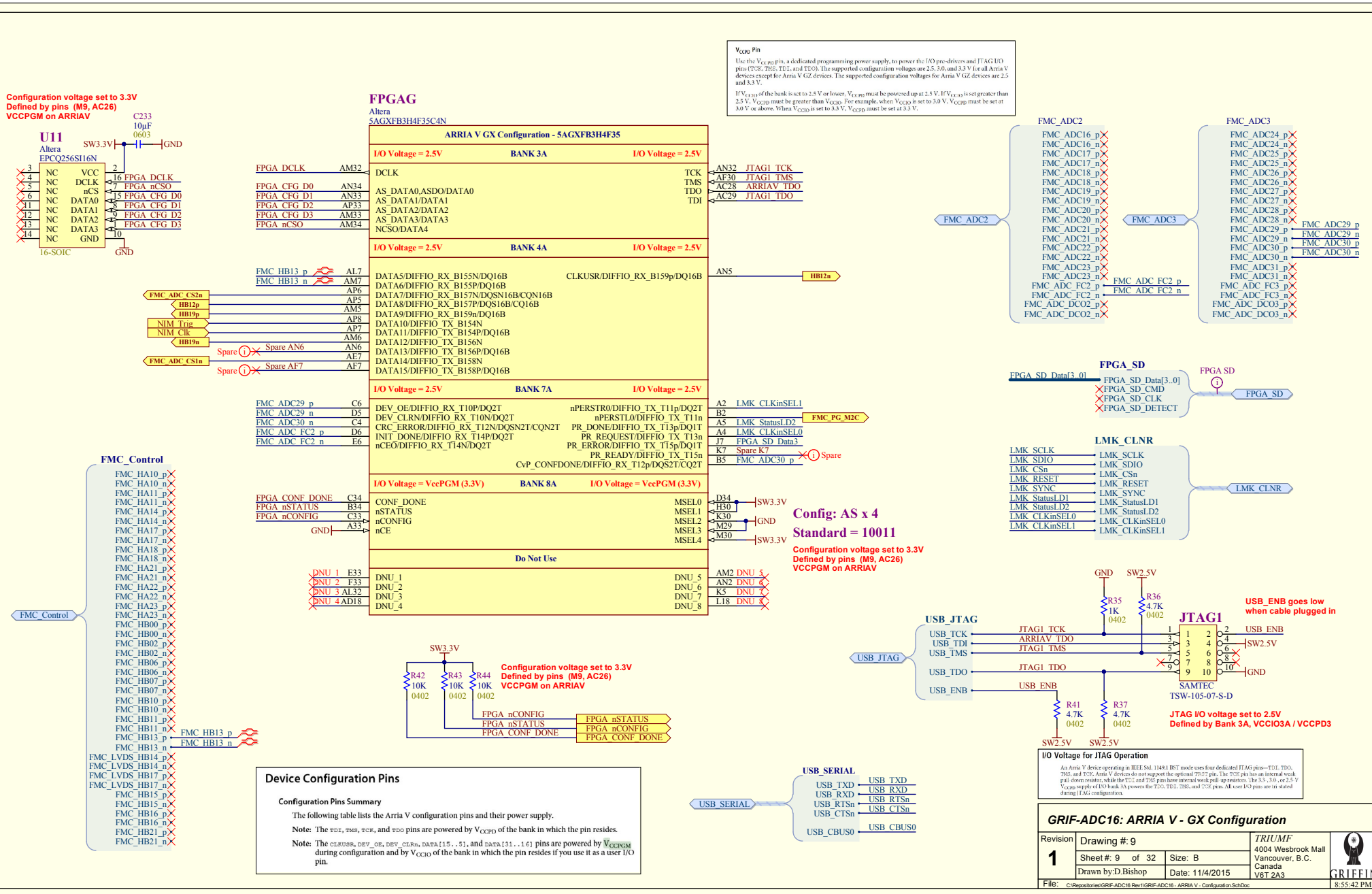

FPGAF
Altera
5AGXFB3H4F35C4N
ARRIA V GX Tranceiver Right Bank - 5AGXFB3H4F35
BANK R0
BANK R1
Reference Resistor
GB_RX
GB_TX
FMC_GBXCVR
FMC_Control
Rref2
2.0K
0402
GND
RREF_BR
REFCLK0Rp
REFCLK0Rn
REFCLK1Rp
REFCLK1Rn
REFCLK2Rp
REFCLK2Rn
REFCLK3Rp
REFCLK3Rn
Spare CLK In
Spare GB_RX10p
Spare GB_RX10n
Spare GB_RX11p
Spare GB_RX11n
NoVIA_GB_RX8p
NoVIA_GB_RX8n
NoVIA_GB_RX9p
NoVIA_GB_RX9n
FPGA_ClnClk2_P
FPGA_ClnClk2_N
GBTCLK0_M2C_P
GBTCLK0_M2C_N
GBTCLK1_M2C_P
GBTCLK1_M2C_N
FMC_HB02_p
FMC_HB02_n
GRIF-ADC16: ARRIA V - Transceiver Right Bank
Revision
1
Drawing #: 8
Sheet #: 8 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - Transceiver Right Bank.SchDoc


Configuration voltage set to 3.3V
Defined by pins (M9, AC26)
VCCPGM on ARRIAV
U11
Altera
EPCQ256SI16N
16-SOIC
C233
10µF
0603
SW3.3V
GND
FPGAG
Altera
5AGXFB3H4F35C4N
ARRIA V GX Configuration - 5AGXFB3H4F35
I/O Voltage = 2.5V
BANK 3A
BANK 4A
BANK 7A
I/O Voltage = VccPGM (3.3V)
BANK 8A
Do Not Use
DCLK
AS_DATA0/ASDO/DATA0
AS_DATA1/DATA1
AS_DATA2/DATA2
AS_DATA3/DATA3
NCSO/DATA4
TCK
TMS
TDO
TDI
JTAG1_TCK
JTAG1_TMS
ARRIAV_TDO
JTAG1_TDO
CONF_DONE
nSTATUS
nCONFIG
nCE
MSEL0
MSEL1
MSEL2
MSEL3
MSEL4
Config: AS x 4
Standard = 10011
Configuration voltage set to 3.3V
Defined by pins (M9, AC26)
VCCPGM on ARRIAV
VCCPD Pin
FMC_ADC2
FMC_ADC3
FPGA_SD
LMK_CLNR
FMC_Control
USB_JTAG
JTAG1
USB_ENB goes low
when cable plugged in
SAMTEC
TSW-105-07-S-D
JTAG I/O voltage set to 2.5V
Defined by Bank 3A, VCCIO3A / VCCPD3
USB_SERIAL
Device Configuration Pins
Configuration Pins Summary
I/O Voltage for JTAG Operation
GRIF-ADC16: ARRIA V - GX Configuration
Revision
1
Drawing #: 9
Sheet #: 9 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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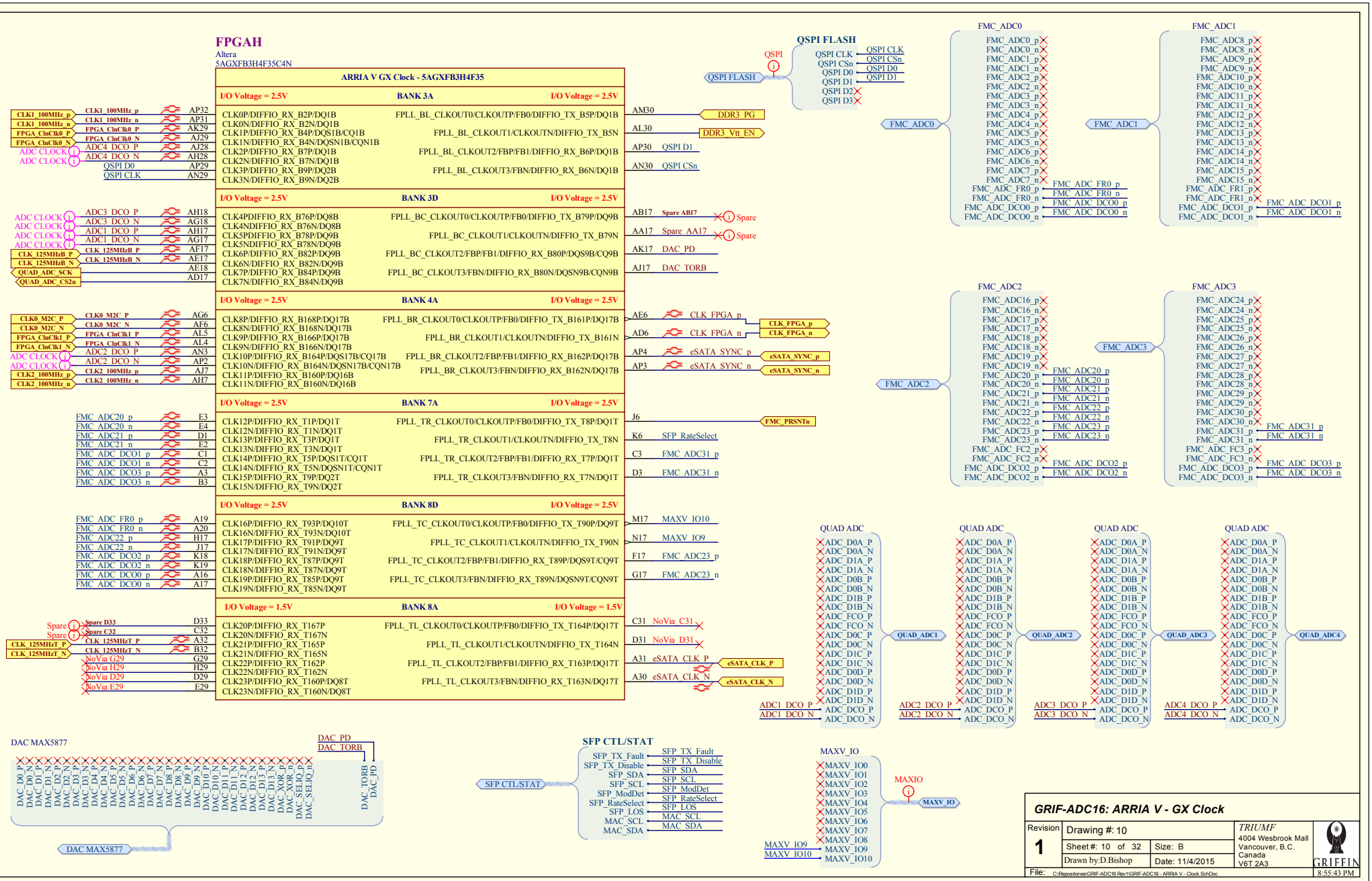
FPGAH
Altera
5AGXFB3H4F35C4N
ARRIA V GX Clock - 5AGXFB3H4F35
I/O Voltage = 2.5V
BANK 3A
I/O Voltage = 2.5V
CLK0P/DIFFIO_RX_B2P/DQ1B
CLK0N/DIFFIO_RX_B2N/DQ1B
CLK1P/DIFFIO_RX_B4P/DQS1B/CQ1B
CLK1N/DIFFIO_RX_B4N/DQSN1B/CQN1B
CLK2P/DIFFIO_RX_B7P/DQ1B
CLK2N/DIFFIO_RX_B7N/DQ1B
CLK3P/DIFFIO_RX_B9P/DQ2B
CLK3N/DIFFIO_RX_B9N/DQ2B
FPLL_BL_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_B5P/DQ1B
FPLL_BL_CLKOUT1/CLKOUTN/DIFFIO_TX_B5N
FPLL_BL_CLKOUT2/FBP/FB1/DIFFIO_RX_B6P/DQ1B
FPLL_BL_CLKOUT3/FBN/DIFFIO_RX_B6N/DQ1B
I/O Voltage = 2.5V
BANK 3D
I/O Voltage = 2.5V
CLK4PDIFFIO_RX_B76P/DQ8B
CLK4NDIFFIO_RX_B76N/DQ8B
CLK5PDIFFIO_RX_B78P/DQ9B
CLK5NDIFFIO_RX_B78N/DQ9B
CLK6P/DIFFIO_RX_B82P/DQ9B
CLK6N/DIFFIO_RX_B82N/DQ9B
CLK7P/DIFFIO_RX_B84P/DQ9B
CLK7N/DIFFIO_RX_B84N/DQ9B
FPLL_BC_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_B79P/DQ9B
FPLL_BC_CLKOUT1/CLKOUTN/DIFFIO_TX_B79N
FPLL_BC_CLKOUT2/FBP/FB1/DIFFIO_RX_B80P/DQS9B/CQ9B
FPLL_BC_CLKOUT3/FBN/DIFFIO_RX_B80N/DQSN9B/CQN9B
I/O Voltage = 2.5V
BANK 4A
I/O Voltage = 2.5V
CLK8P/DIFFIO_RX_B168P/DQ17B
CLK8N/DIFFIO_RX_B168N/DQ17B
CLK9P/DIFFIO_RX_B166P/DQ17B
CLK9N/DIFFIO_RX_B166N/DQ17B
CLK10P/DIFFIO_RX_B164P/DQS17B/CQ17B
CLK10N/DIFFIO_RX_B164N/DQSN17B/CQN17B
CLK11P/DIFFIO_RX_B160P/DQ16B
CLK11N/DIFFIO_RX_B160N/DQ16B
FPLL_BR_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_B161P/DQ17B
FPLL_BR_CLKOUT1/CLKOUTN/DIFFIO_TX_B161N
FPLL_BR_CLKOUT2/FBP/FB1/DIFFIO_RX_B162P/DQ17B
FPLL_BR_CLKOUT3/FBN/DIFFIO_RX_B162N/DQ17B
I/O Voltage = 2.5V
BANK 7A
I/O Voltage = 2.5V
CLK12P/DIFFIO_RX_T1P/DQ1T
CLK12N/DIFFIO_RX_T1N/DQ1T
CLK13P/DIFFIO_RX_T3P/DQ1T
CLK13N/DIFFIO_RX_T3N/DQ1T
CLK14P/DIFFIO_RX_T5P/DQS1T/CQ1T
CLK14N/DIFFIO_RX_T5N/DQSN1T/CQN1T
CLK15P/DIFFIO_RX_T9P/DQ2T
CLK15N/DIFFIO_RX_T9N/DQ2T
FPLL_TR_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_T8P/DQ1T
FPLL_TR_CLKOUT1/CLKOUTN/DIFFIO_TX_T8N
FPLL_TR_CLKOUT2/FBP/FB1/DIFFIO_RX_T7P/DQ1T
FPLL_TR_CLKOUT3/FBN/DIFFIO_RX_T7N/DQ1T
I/O Voltage = 2.5V
BANK 8D
I/O Voltage = 2.5V
CLK16P/DIFFIO_RX_T93P/DQ10T
CLK16N/DIFFIO_RX_T93N/DQ10T
CLK17P/DIFFIO_RX_T91P/DQ9T
CLK17N/DIFFIO_RX_T91N/DQ9T
CLK18P/DIFFIO_RX_T87P/DQ9T
CLK18N/DIFFIO_RX_T87N/DQ9T
CLK19P/DIFFIO_RX_T85P/DQ9T
CLK19N/DIFFIO_RX_T85N/DQ9T
FPLL_TC_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_T90P/DQ9T
FPLL_TC_CLKOUT1/CLKOUTN/DIFFIO_TX_T90N
FPLL_TC_CLKOUT2/FBP/FB1/DIFFIO_RX_T89P/DQS9T/CQ9T
FPLL_TC_CLKOUT3/FBN/DIFFIO_RX_T89N/DQSN9T/CQN9T
I/O Voltage = 1.5V
BANK 8A
I/O Voltage = 1.5V
CLK20P/DIFFIO_RX_T167P
CLK20N/DIFFIO_RX_T167N
CLK21P/DIFFIO_RX_T165P
CLK21N/DIFFIO_RX_T165N
CLK22P/DIFFIO_RX_T162P
CLK22N/DIFFIO_RX_T162N
CLK23P/DIFFIO_RX_T160P/DQ8T
CLK23N/DIFFIO_RX_T160N/DQ8T
FPLL_TL_CLKOUT0/CLKOUTP/FB0/DIFFIO_TX_T164P/DQ17T
FPLL_TL_CLKOUT1/CLKOUTN/DIFFIO_TX_T164N
FPLL_TL_CLKOUT2/FBP/FB1/DIFFIO_RX_T163P/DQ17T
FPLL_TL_CLKOUT3/FBN/DIFFIO_RX_T163N/DQ17T
QSPI FLASH
QSPI CLK
QSPI CSn
QSPI D0
QSPI D1
QSPI D2
QSPI D3
FMC_ADC0
FMC_ADC1
FMC_ADC2
FMC_ADC3
QUAD ADC
QUAD_ADC1
QUAD_ADC2
QUAD_ADC3
QUAD_ADC4
DAC MAX5877
SFP CTL/STAT
MAXV_IO
MAXIO
GRIF-ADC16: ARRIA V - GX Clock
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
Revision
1
Drawing #: 10
Sheet #: 10 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
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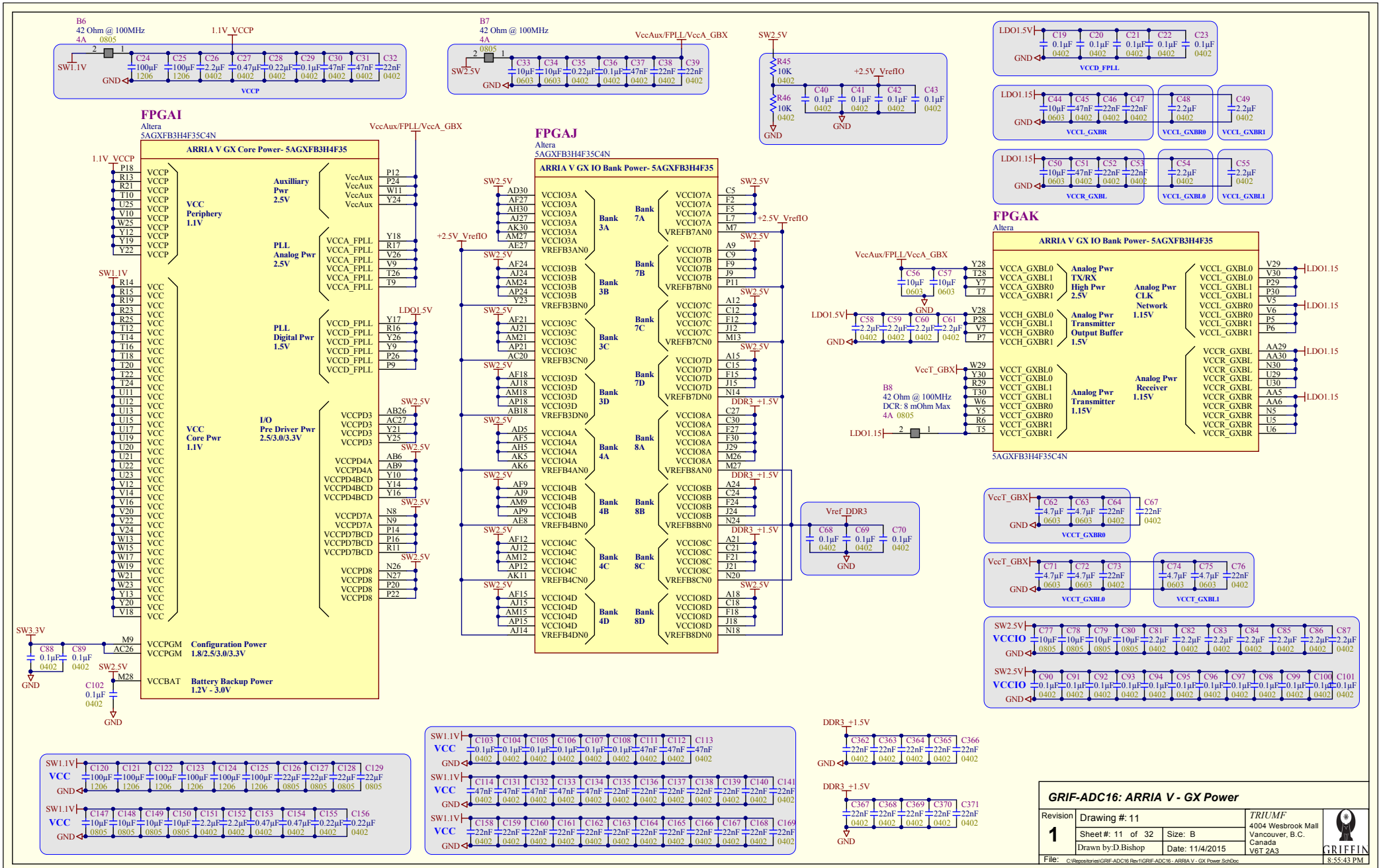
B6
42 Ohm @ 100MHz
4A 0805
1.1V_VCCP
SW1.1V
GND
VCCP
B7
42 Ohm @ 100MHz
4A
VccAux/FPLL/VccA_GBX
SW2.5V
GND
SW2.5V
R45 10K 0402
R46 10K 0402
+2.5V_VrefIO
GND
GND
LDO1.5V
VCCD_FPLL
LDO1.15
VCCL_GXBR
VCCL_GXBR0
VCCL_GXBR1
VCCR_GXBL
VCCL_GXBL0
VCCL_GXBL1
FPGAI
Altera
5AGXFB3H4F35C4N
ARRIA V GX Core Power- 5AGXFB3H4F35
VCC Periphery 1.1V
Auxilliary Pwr 2.5V
PLL Analog Pwr 2.5V
PLL Digital Pwr 1.5V
VCC Core Pwr 1.1V
I/O Pre Driver Pwr 2.5/3.0/3.3V
VCCPGM Configuration Power 1.8/2.5/3.0/3.3V
VCCBAT Battery Backup Power 1.2V - 3.0V
FPGAJ
Altera
5AGXFB3H4F35C4N
ARRIA V GX IO Bank Power- 5AGXFB3H4F35
Bank 3A
Bank 3B
Bank 3C
Bank 3D
Bank 4A
Bank 4B
Bank 4C
Bank 4D
Bank 7A
Bank 7B
Bank 7C
Bank 7D
Bank 8A
Bank 8B
Bank 8C
Bank 8D
+2.5V_VrefIO
DDR3_+1.5V
Vref_DDR3
FPGAK
Altera
ARRIA V GX IO Bank Power- 5AGXFB3H4F35
Analog Pwr TX/RX High Pwr 2.5V
Analog Pwr CLK Network 1.15V
Analog Pwr Transmitter Output Buffer 1.5V
Analog Pwr Transmitter 1.15V
Analog Pwr Receiver 1.15V
B8
42 Ohm @ 100MHz
DCR: 8 mOhm Max
4A 0805
5AGXFB3H4F35C4N
VCCT_GXBR0
VCCT_GXBL0
VCCT_GXBL1
VCCR_GXBL
VCCR_GXBR
SW3.3V
SW2.5V
VCCIO
GRIF-ADC16: ARRIA V - GX Power
Revision 1
Drawing #: 11
Sheet #: 11 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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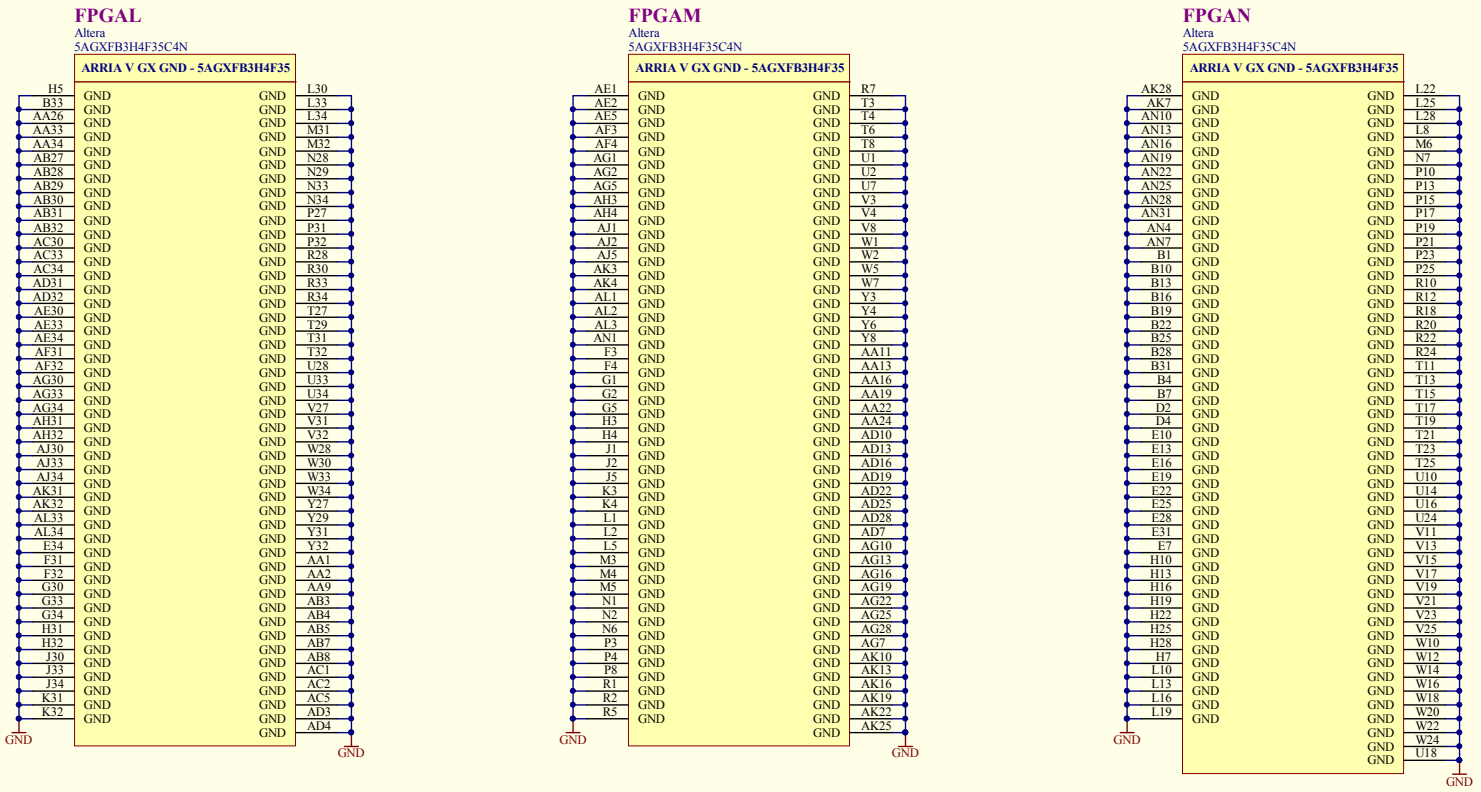
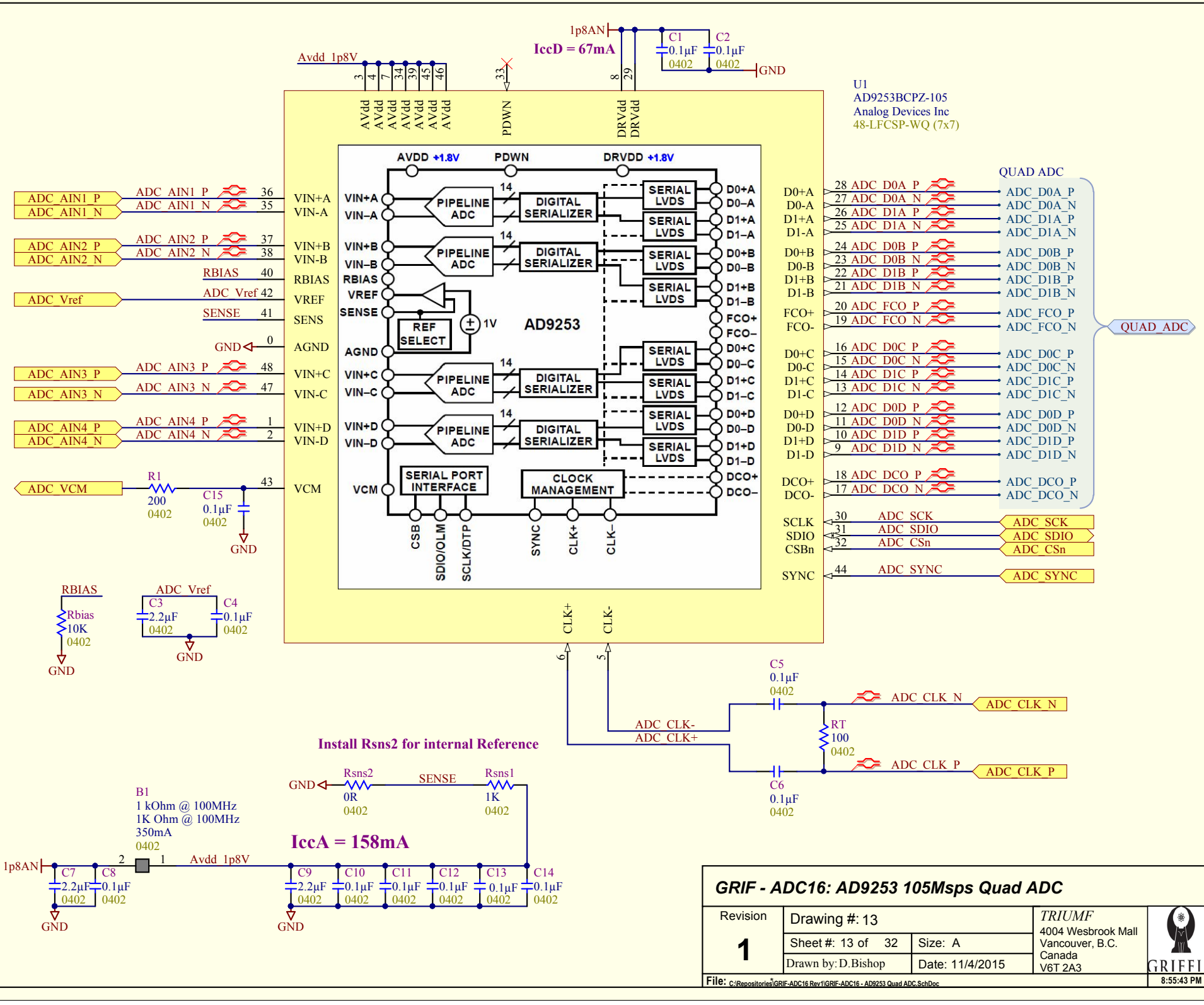


GRIF-ADC16: ARRIA V - GX GND

Revision 1	Drawing #: 12		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 12 of 32	Size: B	
	Drawn by:D.Bishop	Date: 11/4/2015	
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - ARRIA V - GX GND.SchDoc			8:55:43 PM


1p8AN
IccD = 67mA
C1 0.1µF 0402
C2 0.1µF 0402
GND
Avdd_1p8V
U1
AD9253BCPZ-105
Analog Devices Inc
48-LFCSP-WQ (7x7)
AVDD +1.8V
PDWN
DRVDD +1.8V
AD9253
PIPELINE ADC
DIGITAL SERIALIZER
SERIAL LVDS
REF SELECT
SERIAL PORT INTERFACE
CLOCK MANAGEMENT
QUAD ADC
QUAD_ADC
ADC_AIN1_P
ADC_AIN1_N
ADC_AIN2_P
ADC_AIN2_N
ADC_Vref
ADC_AIN3_P
ADC_AIN3_N
ADC_AIN4_P
ADC_AIN4_N
ADC_VCM
R1 200 0402
C15 0.1µF 0402
RBIAS
Rbias 10K 0402
ADC_Vref
C3 2.2µF 0402
C4 0.1µF 0402
CLK+
CLK-
C5 0.1µF 0402
C6 0.1µF 0402
RT 100 0402
ADC_CLK_N
ADC_CLK_P
Install Rsns2 for internal Reference
Rsns2 0R 0402
Rsns1 1K 0402
SENSE
IccA = 158mA
B1
1 kOhm @ 100MHz
1K Ohm @ 100MHz
350mA
0402
C7 2.2µF 0402
C8 0.1µF 0402
C9 2.2µF 0402
C10 0.1µF 0402
C11 0.1µF 0402
C12 0.1µF 0402
C13 0.1µF 0402
C14 0.1µF 0402
GRIF - ADC16: AD9253 105Msps Quad ADC
Revision 1
Drawing #: 13
Sheet #: 13 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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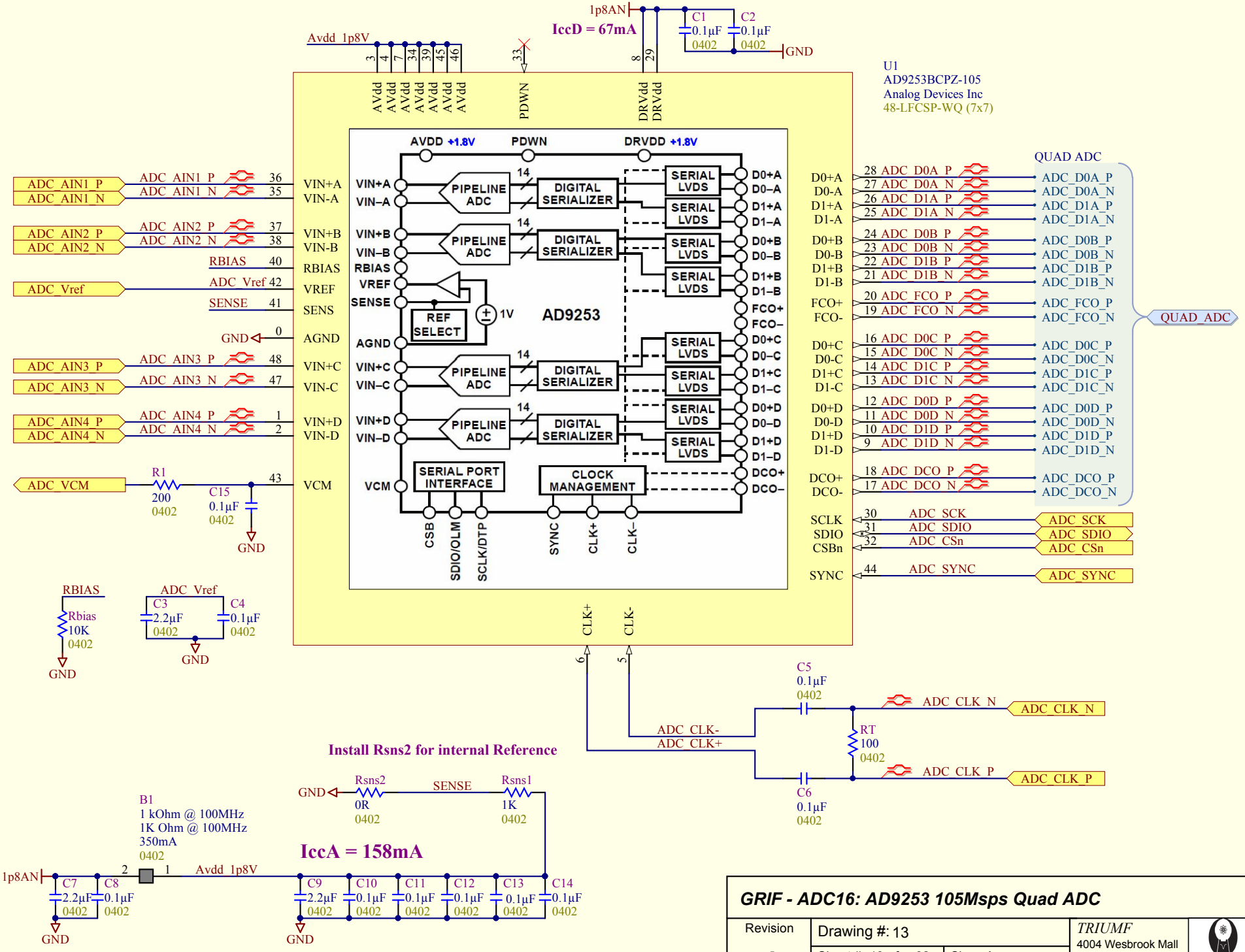
1p8AN
IccD = 67mA
C1 0.1µF 0402
C2 0.1µF 0402
GND
Avdd_1p8V
U1
AD9253BCPZ-105
Analog Devices Inc
48-LFCSP-WQ (7x7)
AVDD +1.8V
PDWN
DRVDD +1.8V
AD9253
PIPELINE ADC
DIGITAL SERIALIZER
SERIAL LVDS
REF SELECT
SERIAL PORT INTERFACE
CLOCK MANAGEMENT
QUAD ADC
QUAD_ADC
ADC_AIN1_P
ADC_AIN1_N
ADC_AIN2_P
ADC_AIN2_N
ADC_Vref
ADC_AIN3_P
ADC_AIN3_N
ADC_AIN4_P
ADC_AIN4_N
ADC_VCM
R1 200 0402
C15 0.1µF 0402
RBIAS
Rbias 10K 0402
ADC_Vref
C3 2.2µF 0402
C4 0.1µF 0402
CLK+
CLK-
C5 0.1µF 0402
C6 0.1µF 0402
RT 100 0402
ADC_CLK_N
ADC_CLK_P
Install Rsns2 for internal Reference
Rsns2 0R 0402
Rsns1 1K 0402
SENSE
B1
1 kOhm @ 100MHz
1K Ohm @ 100MHz
350mA
0402
IccA = 158mA
C7 2.2µF 0402
C8 0.1µF 0402
C9 2.2µF 0402
C10 0.1µF 0402
C11 0.1µF 0402
C12 0.1µF 0402
C13 0.1µF 0402
C14 0.1µF 0402
GRIF - ADC16: AD9253 105Msps Quad ADC
Revision 1
Drawing #: 13
Sheet #: 13 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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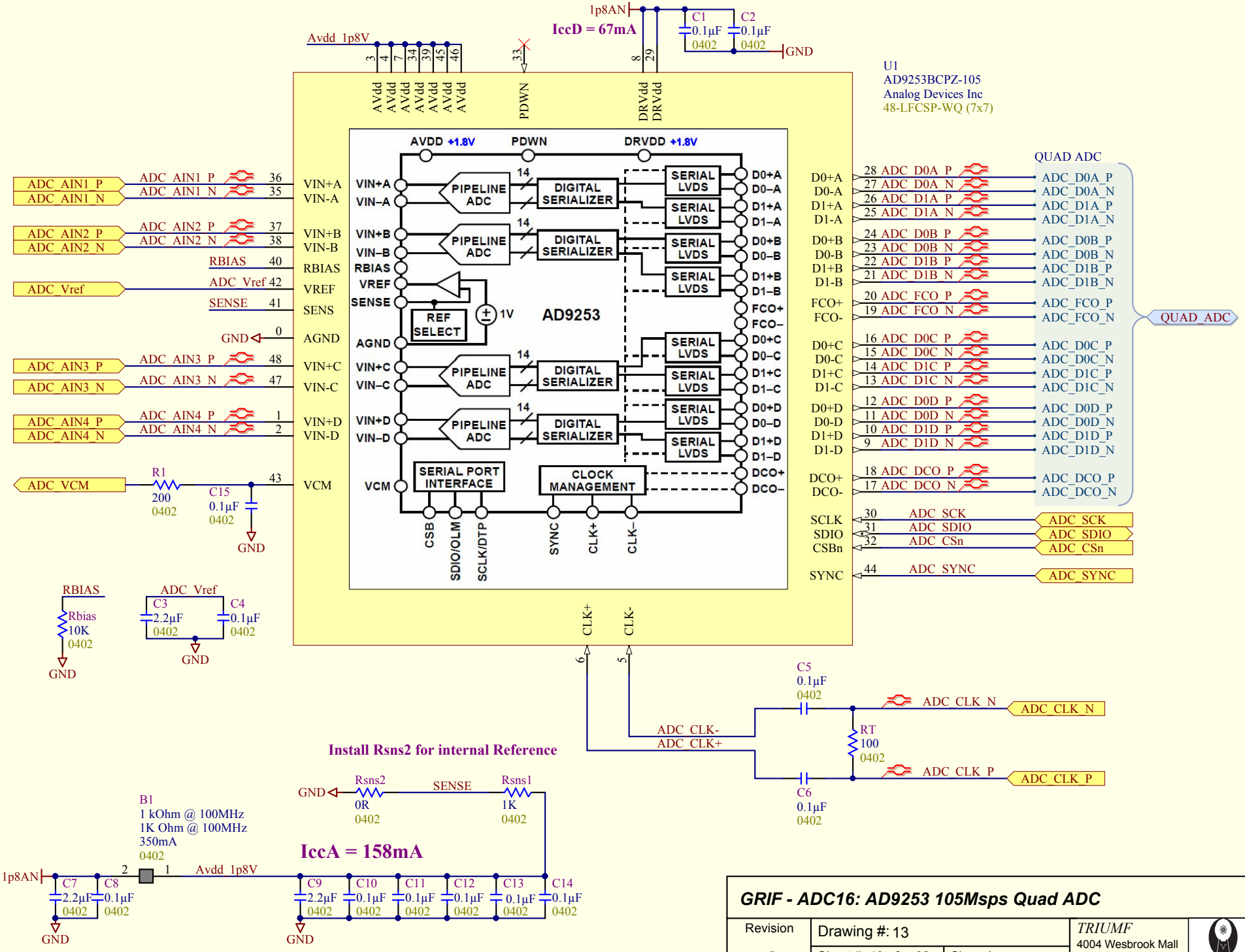
1p8AN
IccD = 67mA
C1 0.1µF 0402
C2 0.1µF 0402
GND
Avdd_1p8V
U1
AD9253BCPZ-105
Analog Devices Inc
48-LFCSP-WQ (7x7)
AVDD +1.8V
PDWN
DRVDD +1.8V
AD9253
PIPELINE ADC
DIGITAL SERIALIZER
SERIAL LVDS
REF SELECT
SERIAL PORT INTERFACE
CLOCK MANAGEMENT
QUAD ADC
QUAD_ADC
ADC_AIN1_P
ADC_AIN1_N
ADC_AIN2_P
ADC_AIN2_N
ADC_Vref
ADC_AIN3_P
ADC_AIN3_N
ADC_AIN4_P
ADC_AIN4_N
ADC_VCM
R1 200 0402
C15 0.1µF 0402
RBIAS
Rbias 10K 0402
ADC_Vref
C3 2.2µF 0402
C4 0.1µF 0402
CLK+
CLK-
C5 0.1µF 0402
C6 0.1µF 0402
RT 100 0402
ADC_CLK_N
ADC_CLK_P
Install Rsns2 for internal Reference
Rsns2 0R 0402
Rsns1 1K 0402
SENSE
B1
1 kOhm @ 100MHz
1K Ohm @ 100MHz
350mA
0402
IccA = 158mA
C7 2.2µF 0402
C8 0.1µF 0402
C9 2.2µF 0402
C10 0.1µF 0402
C11 0.1µF 0402
C12 0.1µF 0402
C13 0.1µF 0402
C14 0.1µF 0402
GRIF - ADC16: AD9253 105Msps Quad ADC
Revision 1
Drawing #: 13
Sheet #: 13 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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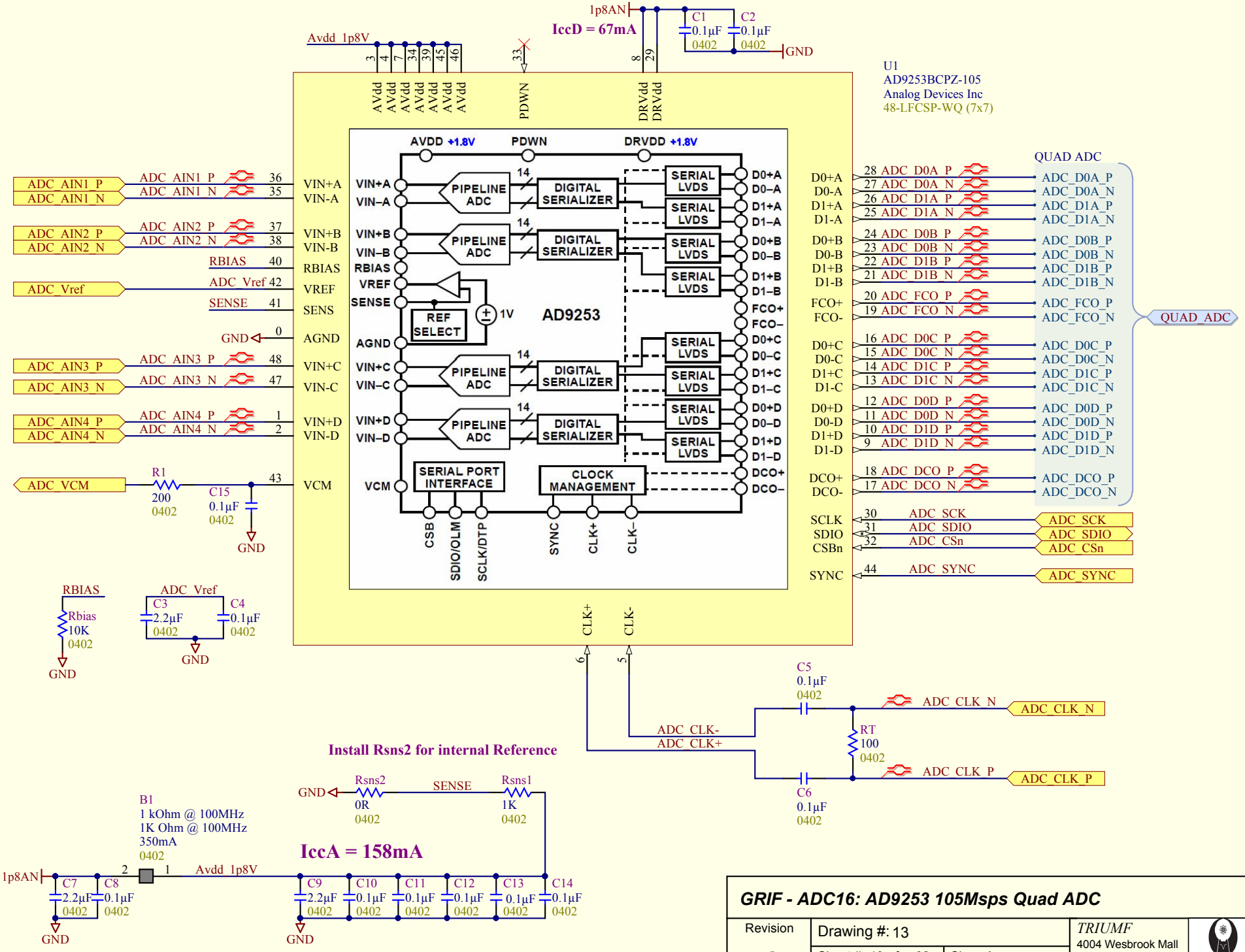
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IccD = 67mA
C1 0.1µF 0402
C2 0.1µF 0402
GND
Avdd_1p8V
U1
AD9253BCPZ-105
Analog Devices Inc
48-LFCSP-WQ (7x7)
AVDD +1.8V
PDWN
DRVDD +1.8V
AD9253
PIPELINE ADC
DIGITAL SERIALIZER
SERIAL LVDS
REF SELECT
SERIAL PORT INTERFACE
CLOCK MANAGEMENT
QUAD ADC
QUAD_ADC
ADC_AIN1_P
ADC_AIN1_N
ADC_AIN2_P
ADC_AIN2_N
ADC_Vref
ADC_AIN3_P
ADC_AIN3_N
ADC_AIN4_P
ADC_AIN4_N
ADC_VCM
R1 200 0402
C15 0.1µF 0402
RBIAS
Rbias 10K 0402
ADC_Vref
C3 2.2µF 0402
C4 0.1µF 0402
CLK+
CLK-
C5 0.1µF 0402
C6 0.1µF 0402
RT 100 0402
ADC_CLK_N
ADC_CLK_P
Install Rsns2 for internal Reference
Rsns2 0R 0402
Rsns1 1K 0402
SENSE
B1
1 kOhm @ 100MHz
1K Ohm @ 100MHz
350mA
0402
IccA = 158mA
C7 2.2µF 0402
C8 0.1µF 0402
C9 2.2µF 0402
C10 0.1µF 0402
C11 0.1µF 0402
C12 0.1µF 0402
C13 0.1µF 0402
C14 0.1µF 0402
GRIF - ADC16: AD9253 105Msps Quad ADC
Revision 1
Drawing #: 13
Sheet #: 13 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
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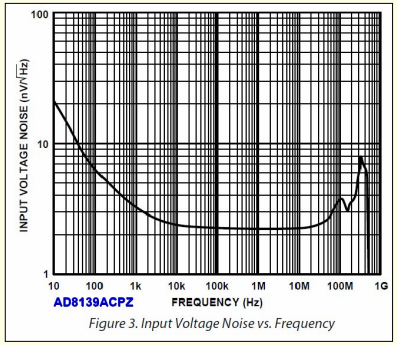

Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter

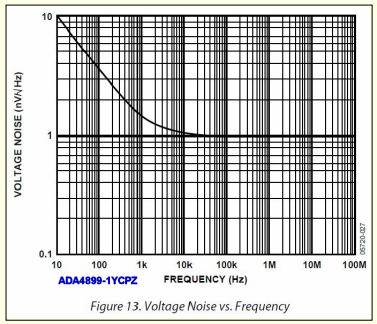

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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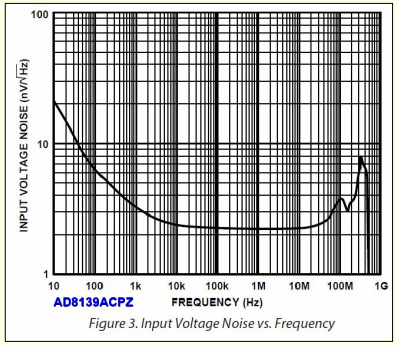
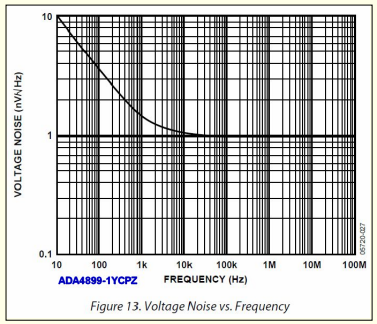


Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter



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ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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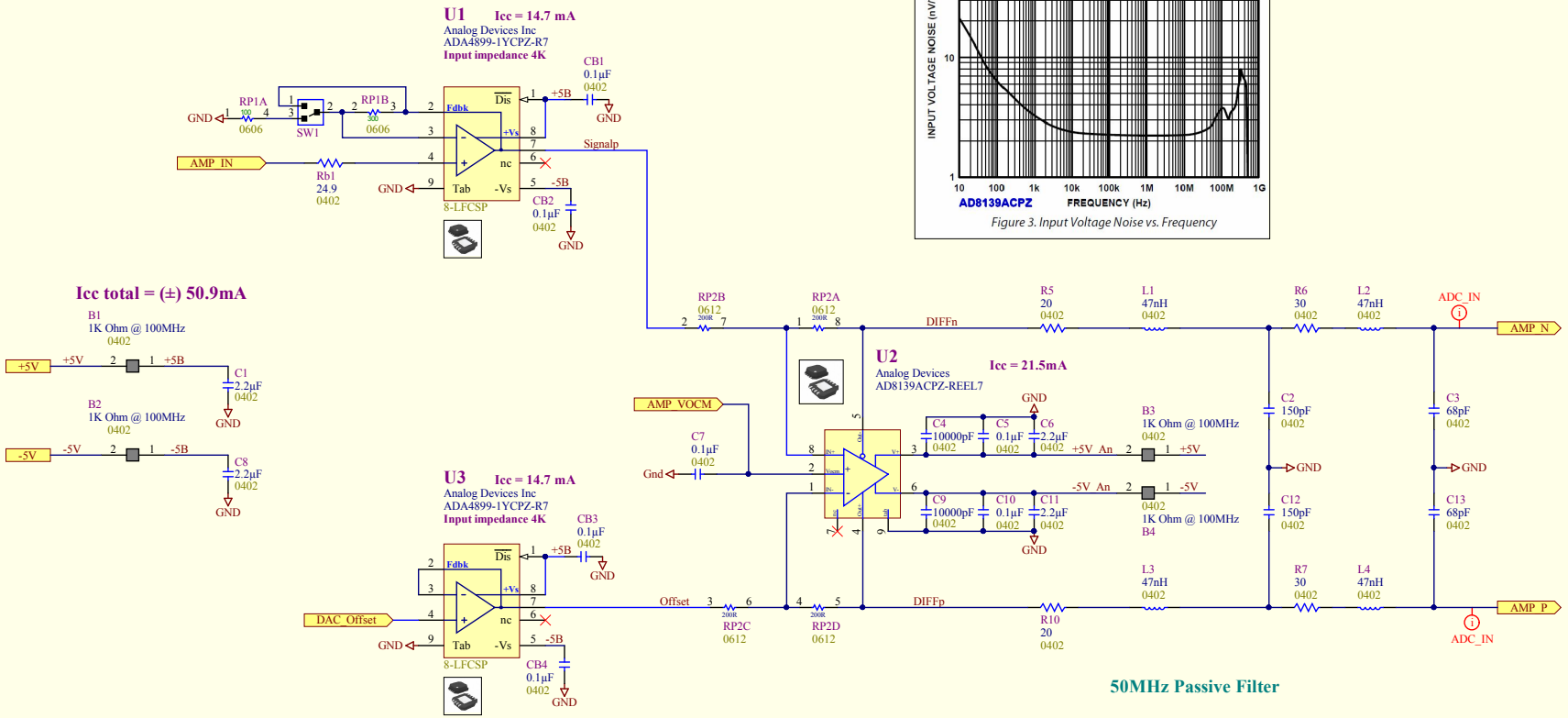

Figure 3. Input Voltage Noise vs. Frequency

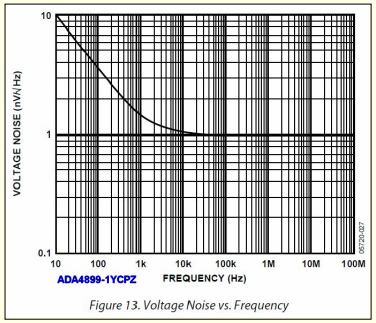

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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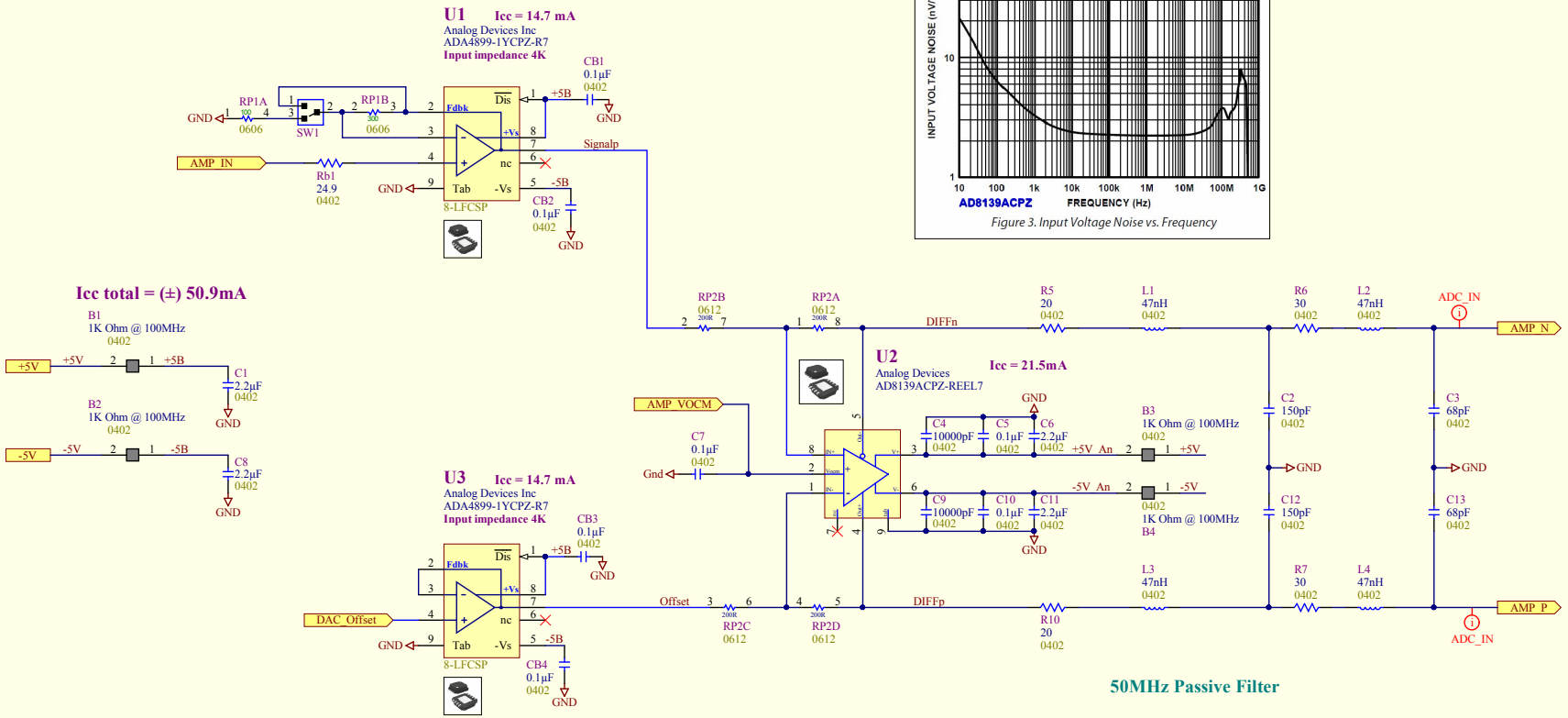

Figure 3. Input Voltage Noise vs. Frequency

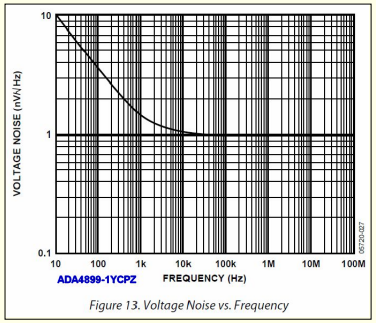

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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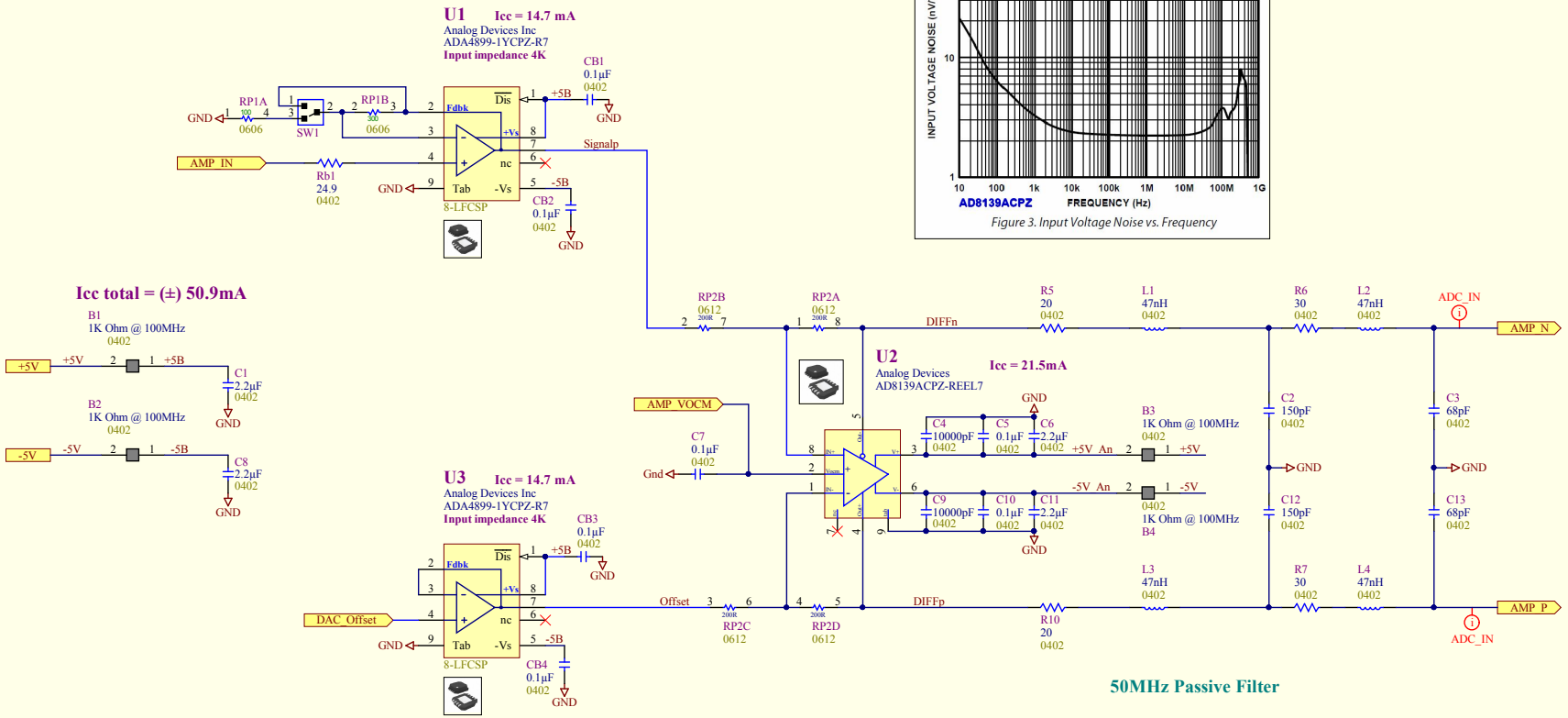

Figure 3. Input Voltage Noise vs. Frequency

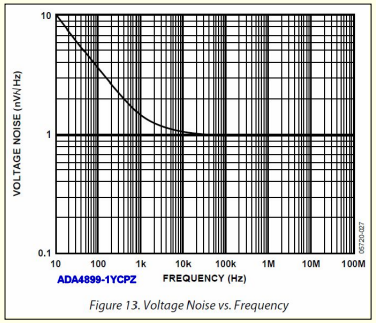

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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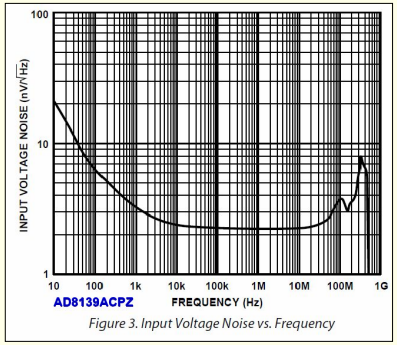
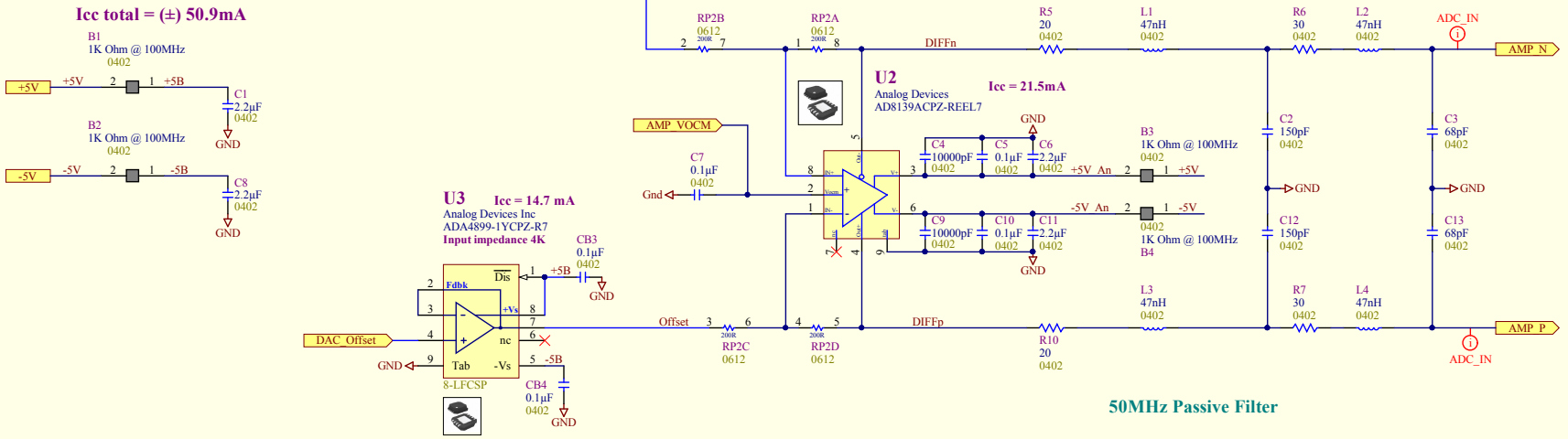


Figure 3. Input Voltage Noise vs. Frequency



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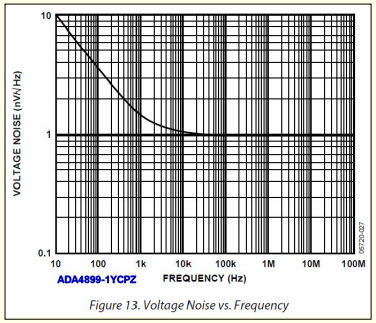

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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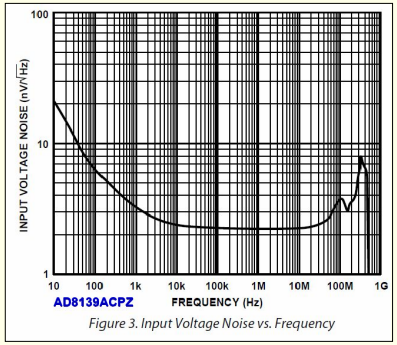
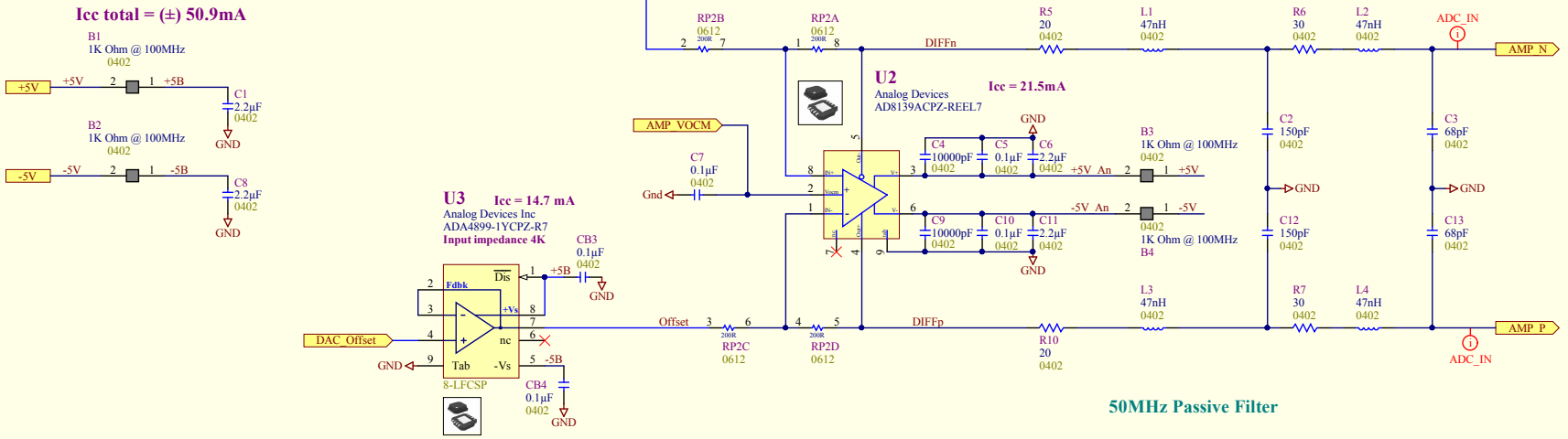


Figure 3. Input Voltage Noise vs. Frequency



50MHz Passive Filter

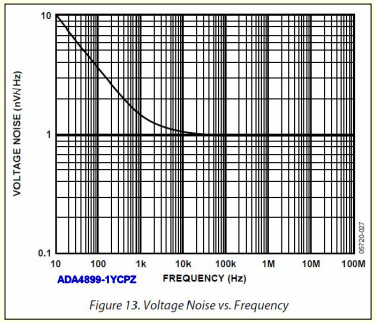


Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

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ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
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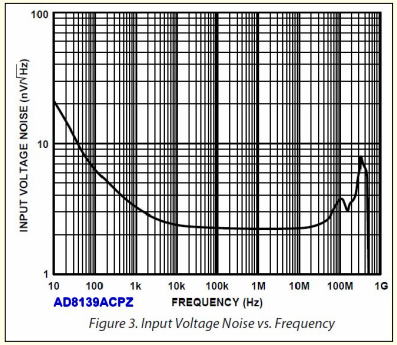
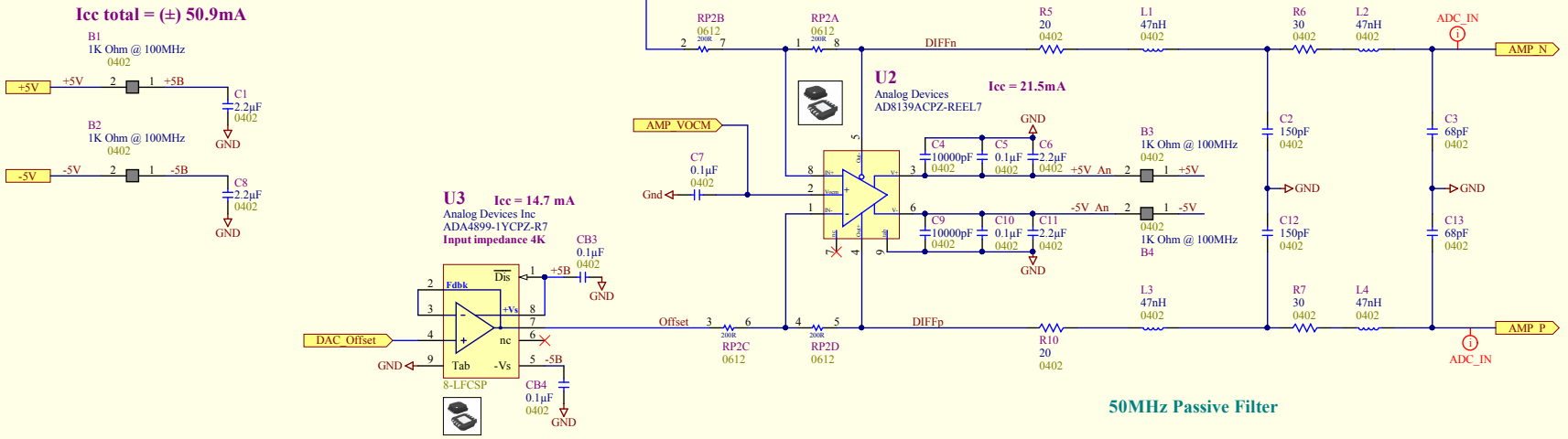


Figure 3. Input Voltage Noise vs. Frequency



50MHz Passive Filter

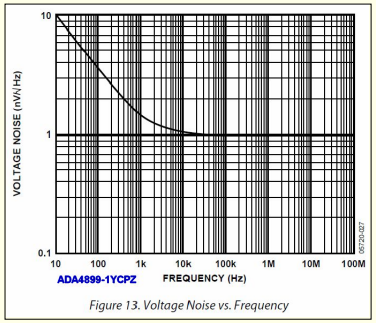


Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 14 of 32	Size: B	
	Drawn by:D.Bishop	Date: 11/4/2015	
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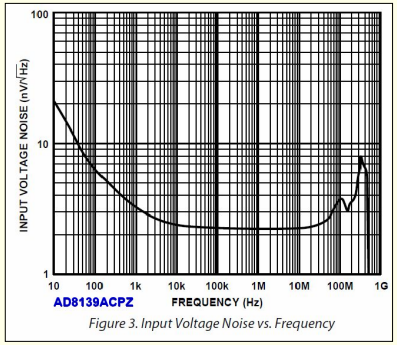

Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter

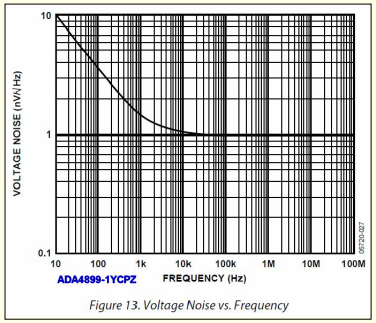

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

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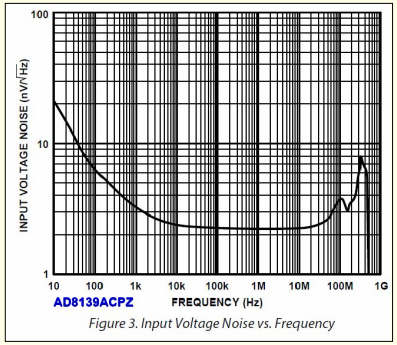

Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter

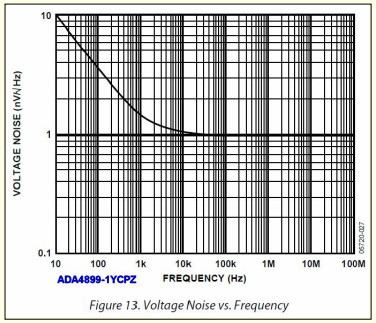

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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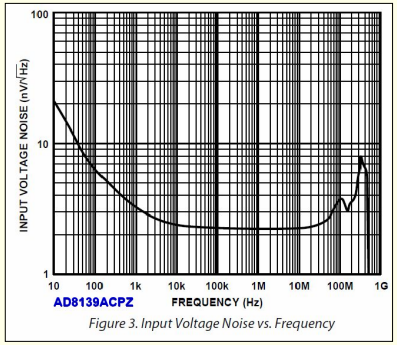

Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter

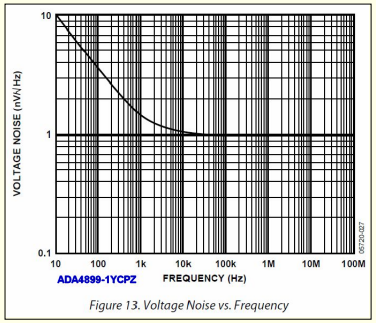

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

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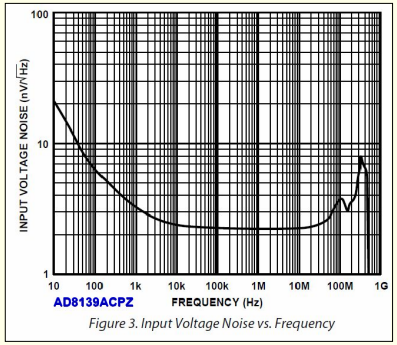

Figure 3. Input Voltage Noise vs. Frequency

50MHz Passive Filter

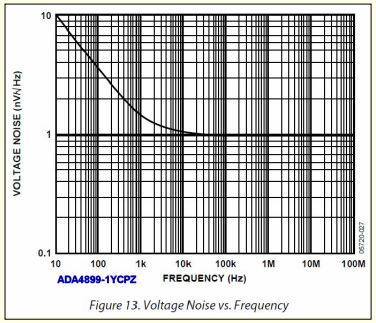

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

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ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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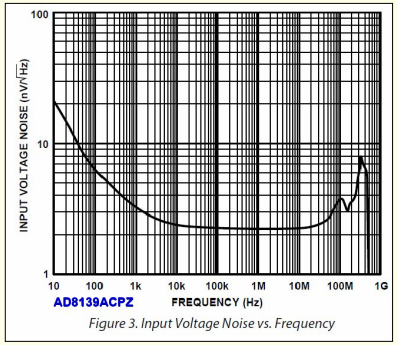

Figure 3. Input Voltage Noise vs. Frequency

U1 **Icc = 14.7 mA**
Analog Devices Inc
ADA4899-1YCPZ-R7
Input impedance 4K

Icc total = (±) 50.9mA

U2 **Icc = 21.5mA**
Analog Devices
AD8139ACPZ-REEL7

U3 **Icc = 14.7 mA**
Analog Devices Inc
ADA4899-1YCPZ-R7
Input impedance 4K

50MHz Passive Filter

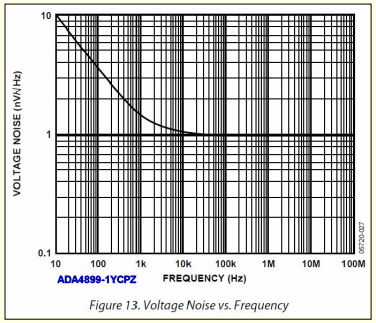

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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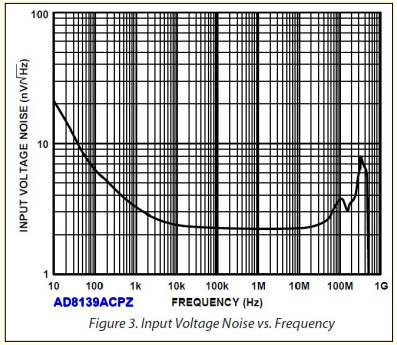

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AD8139ACPZ-REEL7

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Analog Devices Inc
ADA4899-1YCPZ-R7
Input impedance 4K

50MHz Passive Filter

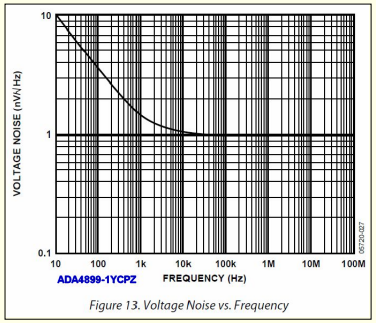

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

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ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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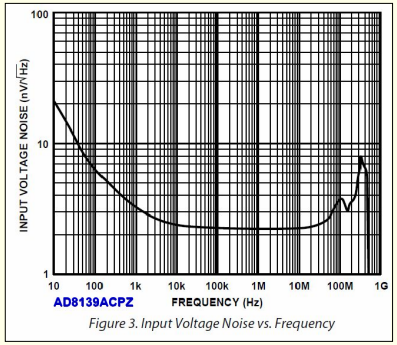

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AD8139ACPZ-REEL7

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Analog Devices Inc
ADA4899-1YCPZ-R7
Input impedance 4K

50MHz Passive Filter

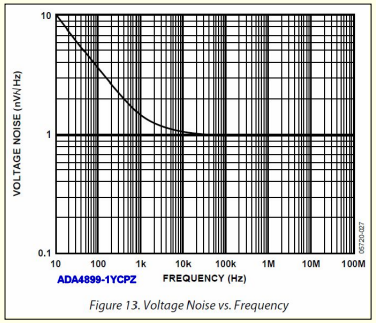

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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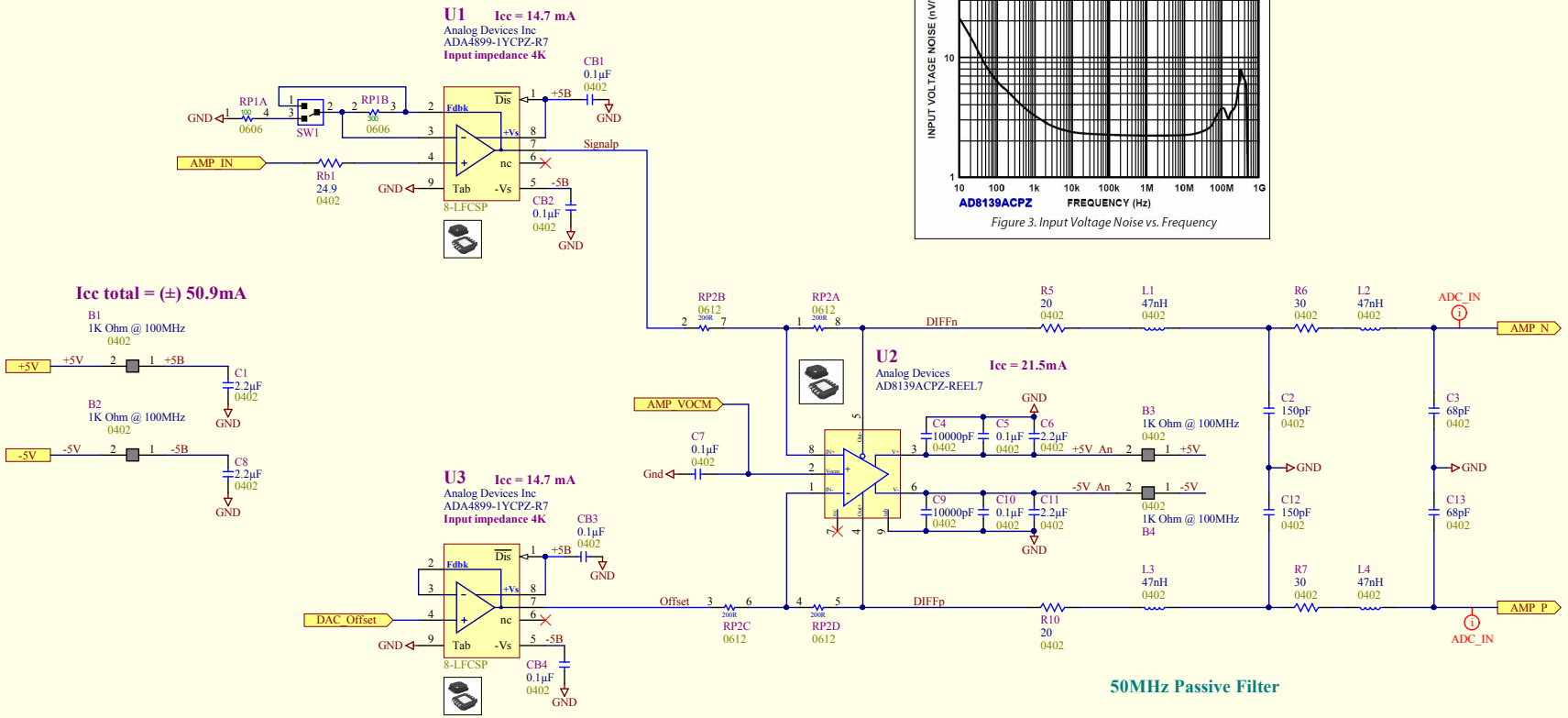

Figure 3. Input Voltage Noise vs. Frequency

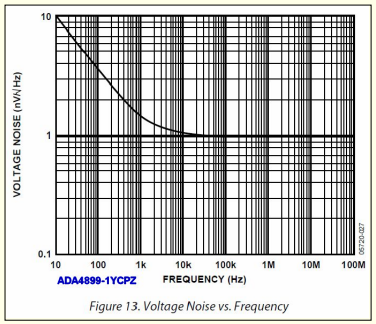

Figure 13. Voltage Noise vs. Frequency

4 resistors - 200 ohms, 0612 package

Vishay Beyschlag - Precision Series (Avnet Express)

ACASA2000S2000P1 (15ppm Rel)	ACAS 0612 200R S 200R P1 (15ppm Rel)
ACASA2000S2000P5 (15ppm Rel)	ACAS 0612 200R S 200R P5 (15ppm Rel)
ACASA2000T2000P1 (10ppm Rel)	ACAS 0612 200R T 200R P1 (10ppm Rel)
ACASA2000ST000P5 (10ppm Rel)	ACAS 0612 200R T 200R P5 (10ppm Rel)
ACASA2000U2000P1 (5ppm Rel)	ACAS 0612 200R U 200R P1 (5ppm Rel)
ACASA2000U2000P5 (5ppm Rel)	ACAS 0612 200R U 200R P5 (5ppm Rel)

Vishay Beyschlag - Professional Series

ACASA200012000P1 (25ppm 0.5%)	ACAS 0612 200R 1 200R P1 (25ppm 0.5%)
ACASA200012000P5 (25ppm 0.5%)	ACAS 0612 200R 1 200R P5 (25ppm 0.5%)
ACASA200022000P1 (50ppm 0.5%)	ACAS 0612 200R 2 200R P1 (50ppm 0.5%)
ACASA200020000P5 (50ppm 0.5%)	ACAS 0612 200R 2 200R P5 (50ppm 0.5%)
ACASA200032000P1 (50ppm 1%)	ACAS 0612 200R 2 200R P1 (50ppm 1%)
ACASA200032000P5 (50ppm 1%)	ACAS 0612 200R 2 200R P5 (50ppm 1%)

GRIF - ADC16 - Front End Amplifiers

Revision 1	Drawing #: 14		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
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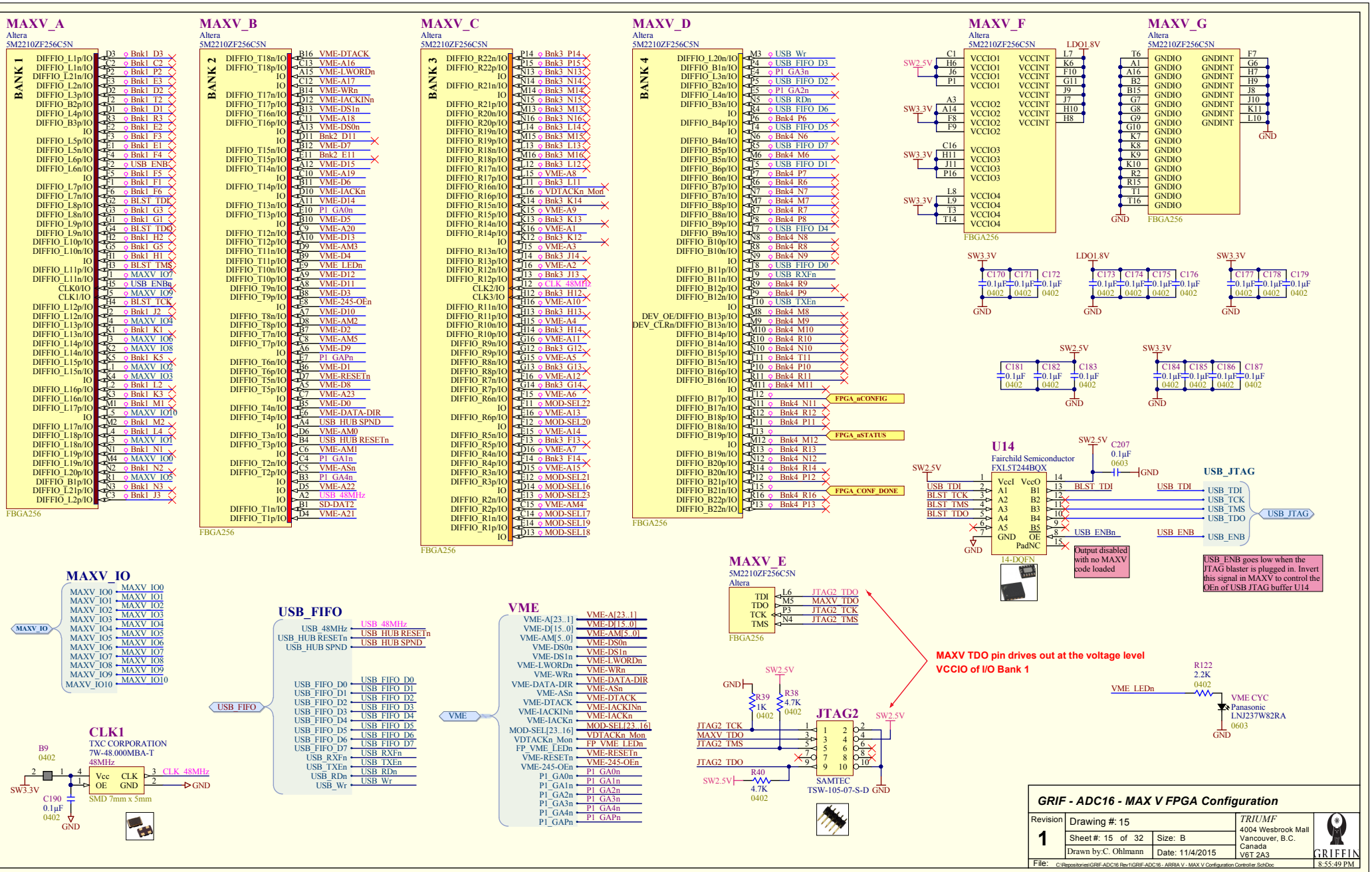
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Altera
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BANK 3
FBGA256
MAXV_D
Altera
5M2210ZF256C5N
BANK 4
FBGA256
FPGA_nCONFIG
FPGA_nSTATUS
FPGA_CONF_DONE
MAXV_F
Altera
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LDO1.8V
FBGA256
MAXV_G
Altera
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FBGA256
U14
Fairchild Semiconductor
FXL5T244BQX
14-DQFN
USB_JTAG
Output disabled with no MAXV code loaded
USB_ENB goes low when the JTAG blaster is plugged in. Invert this signal in MAXV to control the OEn of USB JTAG buffer U14
MAXV_IO
USB_FIFO
VME
MAXV_E
5M2210ZF256C5N
Altera
FBGA256
MAXV TDO pin drives out at the voltage level VCCIO of I/O Bank 1
JTAG2
SAMTEC
TSW-105-07-S-D
CLK1
TXC CORPORATION
7W-48.000MBA-T
48MHz
SMD 7mm x 5mm
VME CYC
Panasonic
LNJ237W82RA
GRIF - ADC16 - MAX V FPGA Configuration
Revision
1
Drawing #: 15
Sheet #: 15 of 32
Size: B
Drawn by:C. Ohlmann
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
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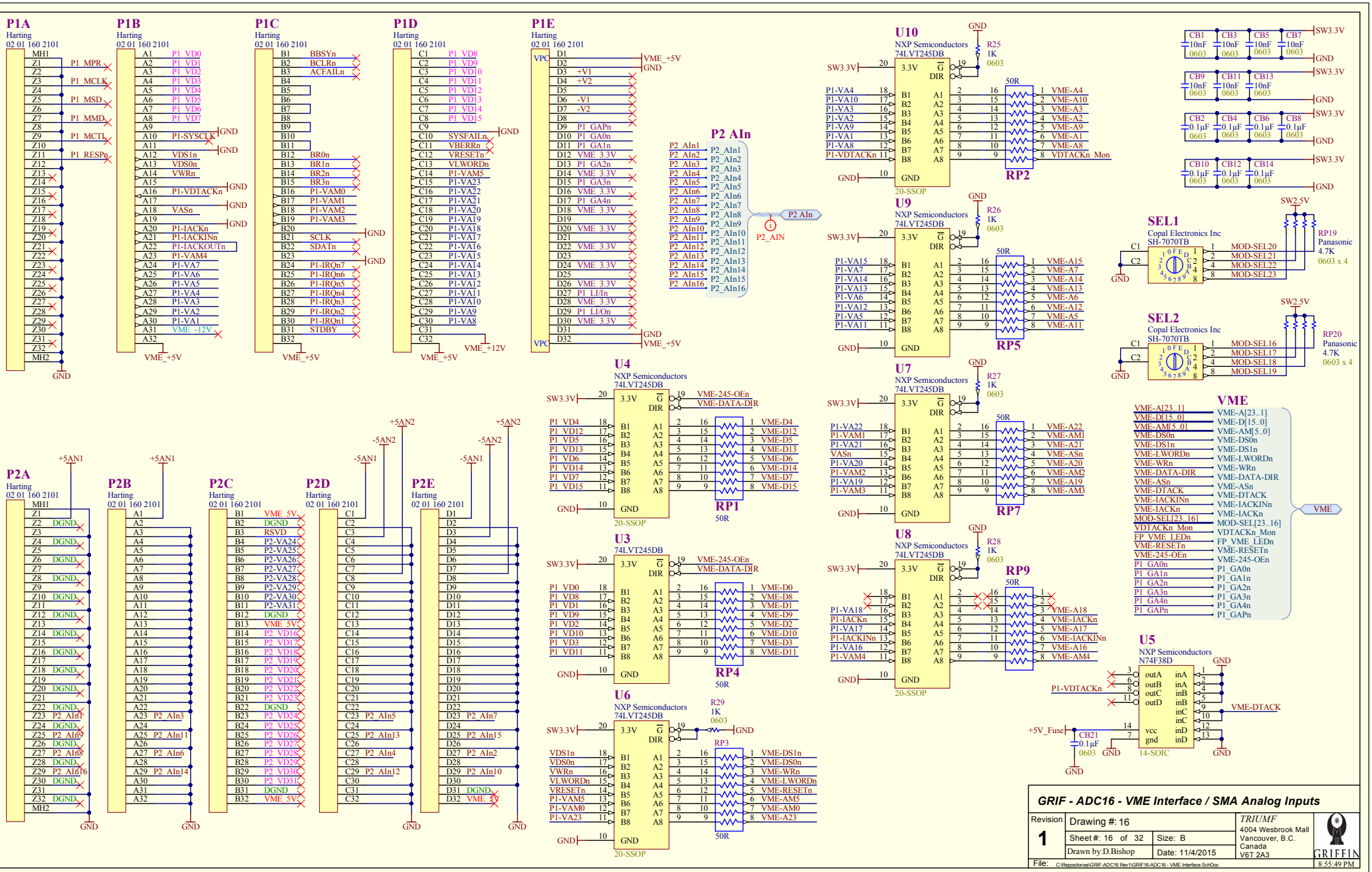
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P1B
Harting
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P1_VD4
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P1_VD6
P1_VD7
P1-SYSCLK
VDS1n
VDS0n
VWRn
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VASn
P1-IACKn
P1-IACKINn
P1-IACKOUTn
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P1-VA7
P1-VA6
P1-VA5
P1-VA4
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Harting
02 01 160 2101
BBSYn
BCLRn
ACFAILn
BR0n
BR1n
BR2n
BR3n
P1-VAM0
P1-VAM1
P1-VAM2
P1-VAM3
SCLK
SDATn
P1-IRQn7
P1-IRQn6
P1-IRQn5
P1-IRQn4
P1-IRQn3
P1-IRQn2
P1-IRQn1
STDBY
VME_+5V
P1D
Harting
02 01 160 2101
P1_VD8
P1_VD9
P1_VD10
P1_VD11
P1_VD12
P1_VD13
P1_VD14
P1_VD15
SYSFAILn
VBERRn
VRESETn
VLWORDn
P1-VAM5
P1-VA23
P1-VA22
P1-VA21
P1-VA20
P1-VA19
P1-VA18
P1-VA17
P1-VA16
P1-VA15
P1-VA14
P1-VA13
P1-VA12
P1-VA11
P1-VA10
P1-VA9
P1-VA8
GND
VME_+12V
VME_+5V
P1E
Harting
02 01 160 2101
VME_+5V
GND
+V1
+V2
-V1
-V2
P1_GAPn
P1_GA0n
P1_GA1n
VME_3.3V
P1_GA2n
P1_GA3n
P1_GA4n
P1_LI/In
P1_LI/On
P2 AIn
P2_AIn1
P2_AIn2
P2_AIn3
P2_AIn4
P2_AIn5
P2_AIn6
P2_AIn7
P2_AIn8
P2_AIn9
P2_AIn10
P2_AIn11
P2_AIn12
P2_AIn13
P2_AIn14
P2_AIn15
P2_AIn16
P2_AIN
P2A
Harting
02 01 160 2101
+5AN1
DGND
P2_AIn1
P2_AIn3
P2_AIn11
P2_AIn8
P2_AIn6
P2_AIn14
P2_AIn16
GND
P2B
Harting
02 01 160 2101
+5AN1
VME_5V
DGND
RSVD
P2-VA24
P2-VA25
P2-VA26
P2-VA27
P2-VA28
P2-VA29
P2-VA30
P2-VA31
VME_5V
P2_VD16
P2_VD17
P2_VD18
P2_VD19
P2_VD20
P2_VD21
P2_VD22
P2_VD23
P2_VD24
P2_VD25
P2_VD26
P2_VD27
P2_VD28
P2_VD29
P2_VD30
P2_VD31
P2C
Harting
02 01 160 2101
-5AN1
+5AN2
-5AN2
P2D
Harting
02 01 160 2101
P2_AIn5
P2_AIn13
P2_AIn4
P2_AIn12
P2E
Harting
02 01 160 2101
P2_AIn7
P2_AIn15
P2_AIn2
P2_AIn10
U4
NXP Semiconductors
74LVT245DB
VME-245-OEn
VME-DATA-DIR
RP1
50R
20-SSOP
U3
NXP Semiconductors
74LVT245DB
RP4
50R
20-SSOP
U6
NXP Semiconductors
74LVT245DB
R29
1K
0603
RP3
50R
20-SSOP
U10
NXP Semiconductors
74LVT245DB
R25
1K
0603
RP2
50R
20-SSOP
U9
NXP Semiconductors
74LVT245DB
R26
1K
0603
RP5
50R
U7
NXP Semiconductors
74LVT245DB
R27
1K
0603
RP7
50R
U8
NXP Semiconductors
74LVT245DB
R28
1K
0603
RP9
50R
20-SSOP
SW3.3V
GND
SEL1
Copal Electronics Inc
SH-7070TB
RP19
Panasonic
4.7K
0603 x 4
SW2.5V
MOD-SEL20
MOD-SEL21
MOD-SEL22
MOD-SEL23
SEL2
Copal Electronics Inc
SH-7070TB
RP20
Panasonic
4.7K
0603 x 4
MOD-SEL16
MOD-SEL17
MOD-SEL18
MOD-SEL19
VME
VME-A[23..1]
VME-D[15..0]
VME-AM[5..0]
VME-DS0n
VME-DS1n
VME-LWORDn
VME-WRn
VME-DATA-DIR
VME-ASn
VME-DTACK
VME-IACKINn
VME-IACKn
MOD-SEL[23..16]
VDTACKn_Mon
FP_VME_LEDn
VME-RESETn
VME-245-OEn
P1_GA0n
P1_GA1n
P1_GA2n
P1_GA3n
P1_GA4n
P1_GAPn
U5
NXP Semiconductors
N74F38D
14-SOIC
VME-DTACK
+5V_Fuse
CB21
0.1µF
0603
CB1
CB3
CB5
CB7
CB9
CB11
CB13
CB2
CB4
CB6
CB8
CB10
CB12
CB14
10nF
0.1µF
GRIF - ADC16 - VME Interface / SMA Analog Inputs
Revision
1
Drawing #: 16
Sheet #: 16 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF16-ADC16 - VME Interface.SchDoc
8:55:49 PM

DDR1A

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

DDR2A

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

MT41J256M16RE-15E IT:D-ND
706-1201-ND

DDR1B

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

+1.5V Idd Max = 2 x 250mA

DDR2B

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

DDR1C

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

(A14 on 4Gb part)

DDR2C

ISSI, Integrated Silicon Solution Inc
IS43TR16128AL-125KBL

(A14 on 4Gb part)

RP6

EXB-2HV560JV

RP8

EXB-2HV560JV

RP10

EXB-2HV560JV

LDO8

Texas Instruments
TPS51200DRCT

10-SON (3x3)

GRIF-ADC16:DDR3 Memory

Revision 1	Drawing #: 17		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 17 of 32	Size: B	
	Drawn by:D.Bishop	Date: 11/4/2015	
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - DDR3 Memory.SchDoc			8:55:50 PM

CLEANER

Texas Instruments
LMK04821NKDT
Clock distribution fanout - 15 channel
64-WQFN (9x9)

LMK04821

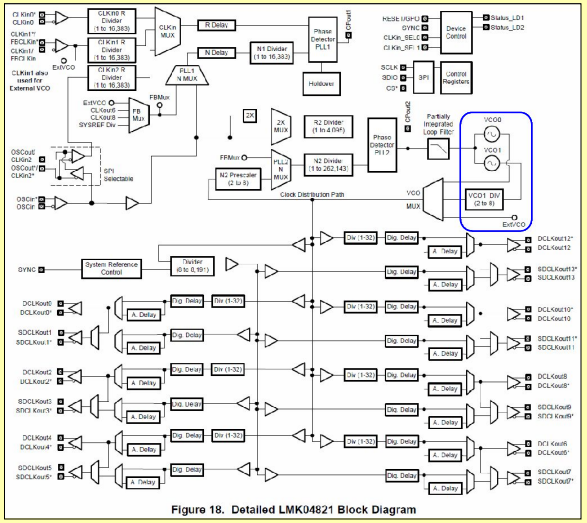

Figure 18. Detailed LMK04821 Block Diagram

OSRAM
LG L29K-G2J1-24-Z

LED9 LED10 LED11 LED12 — 0603 — R48 1K, R49 1K, R50 1K, R51 1K — 0402 — GND

LMK_StatusLD2, LMK_StatusLD1, LMK_CLKinSEL0, LMK_CLKinSEL1, LMK_RESET

R58 1K 0402 — GND

LMK_CSn, LMK_SCLK, LMK_SDIO

CSn, SCK, SDIO, StatusLD2, Status_LD1, CLKin_SEL0, CLKin_SEL1, RESET/GPO, NC7, NC8, NC9

CLN_CLKin0_P / CLN_CLKin0_N — Rt1 100 0402 — Cc1 100nF, Cc2 100nF — 0402 — Clk0_p, Clk0_n — CLKIN0p, CLKIN0n

CLN_CLKin1_P / CLN_CLKin1_N — Rt2 100 0402 — Cc3 100nF, Cc4 100nF — 0402 — Clk1_p, Clk1_n — CLKIN1p/FINp/FBCLKINp, CLKIN1n/FINn/FBCLKINn

CLN_CLKin2_P / CLN_CLKin2_N — Rt3 100 0402 — Cc5 100nF, Cc6 100nF — 0402 — Clk2_p, Clk2_n — CLKIN2p/OSC_OUTp, CLKIN2n/OSC_OUTn

LVDS_VCXO_P / LVDS_VCXO_N — Rt4 100 0402 — Cc7 100nF, Cc8 100nF — 0402 — OSC_p, OSC_n — OSC_INp, OSC_INn

LMK_SYNC — SYNC/SYSREF_REQ

lvds_DCLK_OUT0_p, lvds_DCLK_OUT0_n, lvds_SDCLK_OUT1_p, lvds_SDCLK_OUT1_n — DCLK_OUT0p, DCLK_OUT0n, SDCLK_OUT1p, SDCLK_OUT1n

lvds_DCLK_OUT2_p, lvds_DCLK_OUT2_n, lvds_SDCLK_OUT3_p, lvds_SDCLK_OUT3_n — DCLK_OUT2p, DCLK_OUT2n, SDCLK_OUT3p, SDCLK_OUT3n

lvds_DCLK_OUT4_p, lvds_DCLK_OUT4_n, lvds_SDCLK_OUT5_p, lvds_SDCLK_OUT5_n — DCLK_OUT4p, DCLK_OUT4n, SDCLK_OUT5p, SDCLK_OUT5n

Vcc1_VCO, Vcc2_CG1(Clk1,2), Vcc3_SYSREF, Vcc4_CG2(Clk4,5,6,7), Vcc5_DIG, Vcc6_PLL1, Vcc7_OSCout, Vcc8_OSCin, Vcc9_CP2, Vcc10_PLL2, Vcc11_CG3(Clk8,9,10,11), Vcc12_GC0(Clk0,1,12,13) — +3.3V_VCC1_5_6, +3.3V_VCC2, +3.3V_VCC3, +3.3V_VCC4, +3.3V_VCC7, +3.3V_VCC8_10, +3.3V_VCC9, +3.3V_VCC11, +3.3V_VCC12

LDObyp1, LDObyp2, CPout1, CPout2, DAP — LDO_Byp1, LDO_Byp2, ChargePump1, ChargePump2, GND

C144 10µF 0603, C145 100nF 0402 — GND

Filter for PLL1: Cf6 1nF 0402, Cf5 47nF 0402, Rf3 120K 0402 — GND

Filter for PLL2: Cf8 47pF 0402, Cf7 3900pF 0402, Rf4 680 0402 — GND

DCLK_OUT12p, DCLK_OUT12n, SDCLK_OUT13p, SDCLK_OUT13n — lvds_DCLK_OUT12_p, lvds_DCLK_OUT12_n, lvds_SDCLK_OUT13_p, lvds_SDCLK_OUT13_n — lvds_DCLK_OUT12_p, lvds_DCLK_OUT12_n, lvds_SDCLK_OUT13_p, lvds_SDCLK_OUT13_n

DCLK_OUT10p, DCLK_OUT10n, SDCLK_OUT11p, SDCLK_OUT11n — lvds_DCLK_OUT10_p, lvds_DCLK_OUT10_n, lvds_SDCLK_OUT11_p, lvds_SDCLK_OUT11_n — lvds_DCLK_OUT10_p, lvds_DCLK_OUT10_n, lvds_SDCLK_OUT11_p, lvds_SDCLK_OUT11_n

DCLK_OUT8p, DCLK_OUT8n, SDCLK_OUT9p, SDCLK_OUT9n — lvds_DCLK_OUT8_p, lvds_DCLK_OUT8_n, lvds_SDCLK_OUT9_p, lvds_SDCLK_OUT9_n — lvds_DCLK_OUT8_p, lvds_DCLK_OUT8_n, lvds_SDCLK_OUT9_p, lvds_SDCLK_OUT9_n

DCLK_OUT6p, DCLK_OUT6n, SDCLK_OUT7p, SDCLK_OUT7n — lvds_DCLK_OUT6_p, lvds_DCLK_OUT6_n, lvds_SDCLK_OUT7_p, lvds_SDCLK_OUT7_n — lvds_DCLK_OUT6_p, lvds_DCLK_OUT6_n, lvds_SDCLK_OUT7_p, lvds_SDCLK_OUT7_n

U16

Micrel
SY89544UMG ICC - 50Ma
32-MLF (5x5)

B23 1K Ohm @ 100MHz — SW2.5V 0402 — +2.5_U16

C215 2.2µF 0402, C218 2.2µF 0402, C219 2.2µF 0402 — GND

+2.5_U16 — C109 0.1µF 0402, C110 0.1µF 0402, C206 0.1µF 0402, C220 0.1µF 0402, C221 0.1µF 0402, C222 0.1µF 0402, C225 0.1µF 0402 — GND

Vcc, Vcc, Vcc, Vcc, Vcc, Vcc, Vcc, Vcc, GND, GND, GND, GND, GND, GND, GND, GPAD

4:1 MUX

CLN_CLKin2_CLK0_P / CLN_CLKin2_CLK0_N — IN0, IN0
CLN_CLKin2_CLK1_P / CLN_CLKin2_CLK1_N — IN1, IN1
CLN_CLKin2_CLK2_P / CLN_CLKin2_CLK2_N — IN2, IN2
CLN_CLKin2_CLK3_P / CLN_CLKin2_CLK3_N — IN3, IN3
CLN_CLKin2_Sel0, CLN_CLKin2_Sel1 — SEL0, SEL1
Vt0, Vt1, Vt2, Vt3 — NC, NC — Q, Q — CLKin2_P, CLKin2_N

PD1 2.2K 0402, PD2 2.2K 0402 — GND

LMK_CLNR

LMK_CLNR — LMK_SCLK, LMK_SDIO, LMK_CSn, LMK_RESET, LMK_SYNC, LMK_StatusLD1, LMK_StatusLD2, LMK_CLKinSEL0, LMK_CLKinSEL1

SW3.3V — B17 Ferrite Bead 120 Ohm @ 100MHz 0603 — C157 1µF 0603, C208 100nF 0402, C209 10nF 0402 — +3.3V_VCC8_10 — GND

+3.3V_VCC7 — B25 Ferrite Bead 120 Ohm @ 100MHz 0603 — C226 10nF 0402 — GND

+3.3V_VCC9 — B27 Ferrite Bead 120 Ohm @ 100MHz 0603 — C230 10nF 0402 — GND

SW3.3V — B29 Ferrite Bead 120 Ohm @ 100MHz 0603 — C232 1µF 0603, C312 100nF 0402, C313 10nF 0402, C385 10nF 0402 — +3.3V_VCC1_5_6 — GND

SW3.3V — B14 Ferrite Bead 120 Ohm @ 100MHz 0603 — +3.3V_VCC12 — C146 10nF 0402 — GND

SW3.3V — B24 Ferrite Bead 120 Ohm @ 100MHz 0603 — +3.3V_VCC2 — C214 10nF 0402 — GND

SW3.3V — B26 Ferrite Bead 120 Ohm @ 100MHz 0603 — +3.3V_VCC3 — C229 10nF 0402 — GND

SW3.3V — B28 Ferrite Bead 120 Ohm @ 100MHz 0603 — +3.3V_VCC4 — C231 10nF 0402 — GND

SW3.3V — B30 Ferrite Bead 120 Ohm @ 100MHz 0603 — +3.3V_VCC11 — C314 10nF 0402 — GND

VCXO

VCXO 100MHz LVDS Oscillator
Abracon Corporation
ASG-D-V-A-100.000MHZ
6-SMD (7x5mm)

SW3.3V — B31 Ferrite Bead 120 Ohm @ 100MHz 0603 — C315 1µF 0603, C316 100nF 0603 — +3.3VCXO — GND

ChargePump1 — Vc
+3.3VCXO — OE
VDD, GND, CLK+, CLK- — LVDS_VCXO_P, LVDS_VCXO_N

GRIF - ADC16 - Clock Cleaner - LMK04828/LMK04821

Revision	Drawing #: 18		TRIUMF	Cannot open file TRIUMF.BMP
1	Sheet #: 18 of 32	Size: B	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
	Drawn by: D.Bishop	Date: 11/4/2015		

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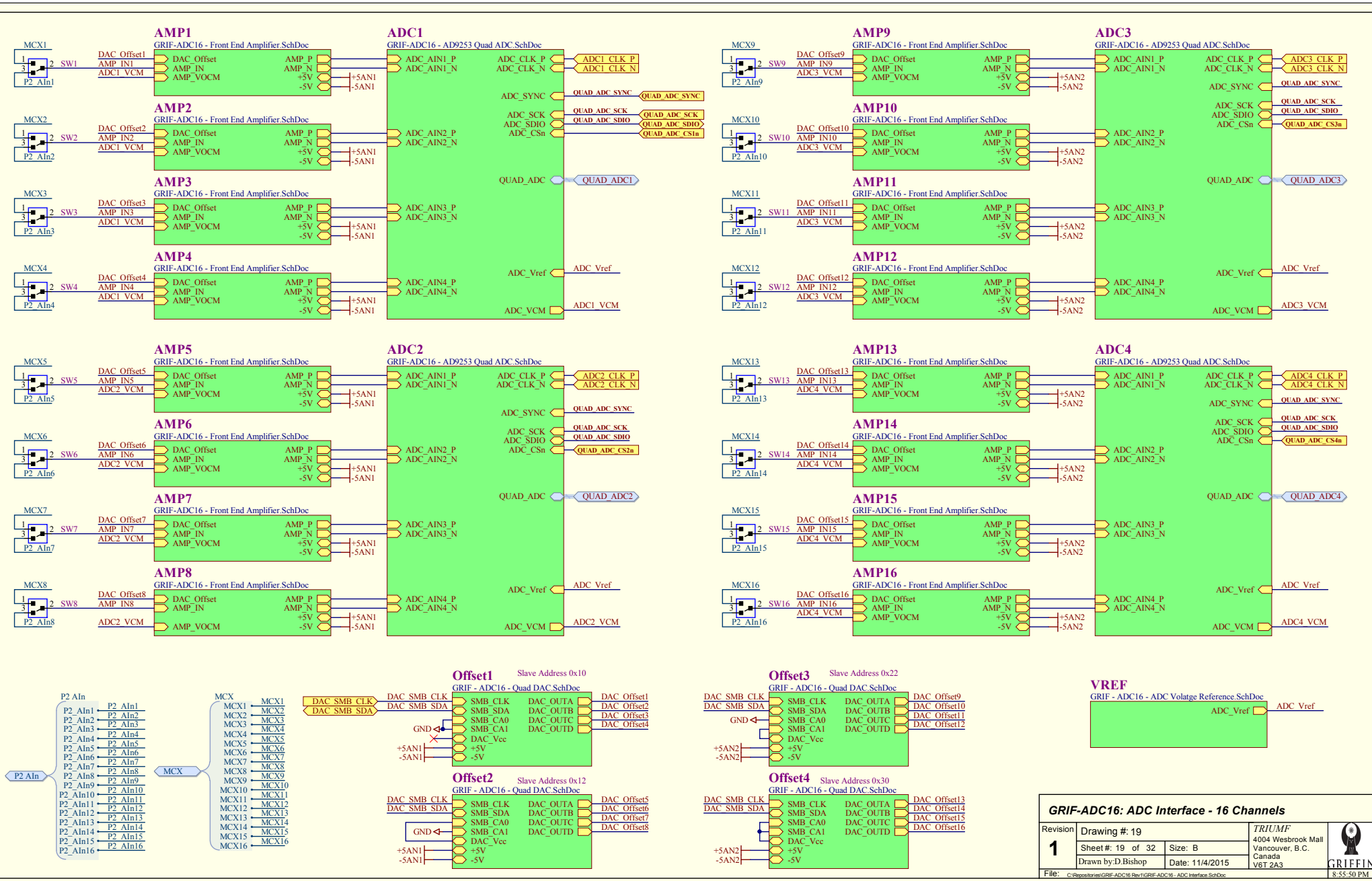
AMP1
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP2
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP3
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP4
GRIF-ADC16 - Front End Amplifier.SchDoc
ADC1
GRIF-ADC16 - AD9253 Quad ADC.SchDoc
AMP5
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP6
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP7
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP8
GRIF-ADC16 - Front End Amplifier.SchDoc
ADC2
GRIF-ADC16 - AD9253 Quad ADC.SchDoc
AMP9
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP10
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP11
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP12
GRIF-ADC16 - Front End Amplifier.SchDoc
ADC3
GRIF-ADC16 - AD9253 Quad ADC.SchDoc
AMP13
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP14
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP15
GRIF-ADC16 - Front End Amplifier.SchDoc
AMP16
GRIF-ADC16 - Front End Amplifier.SchDoc
ADC4
GRIF-ADC16 - AD9253 Quad ADC.SchDoc
Offset1
Slave Address 0x10
GRIF - ADC16 - Quad DAC.SchDoc
Offset2
Slave Address 0x12
GRIF - ADC16 - Quad DAC.SchDoc
Offset3
Slave Address 0x22
GRIF - ADC16 - Quad DAC.SchDoc
Offset4
Slave Address 0x30
GRIF - ADC16 - Quad DAC.SchDoc
VREF
GRIF - ADC16 - ADC Volatge Reference.SchDoc
GRIF-ADC16: ADC Interface - 16 Channels
Revision 1
Drawing #: 19
Sheet #: 19 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
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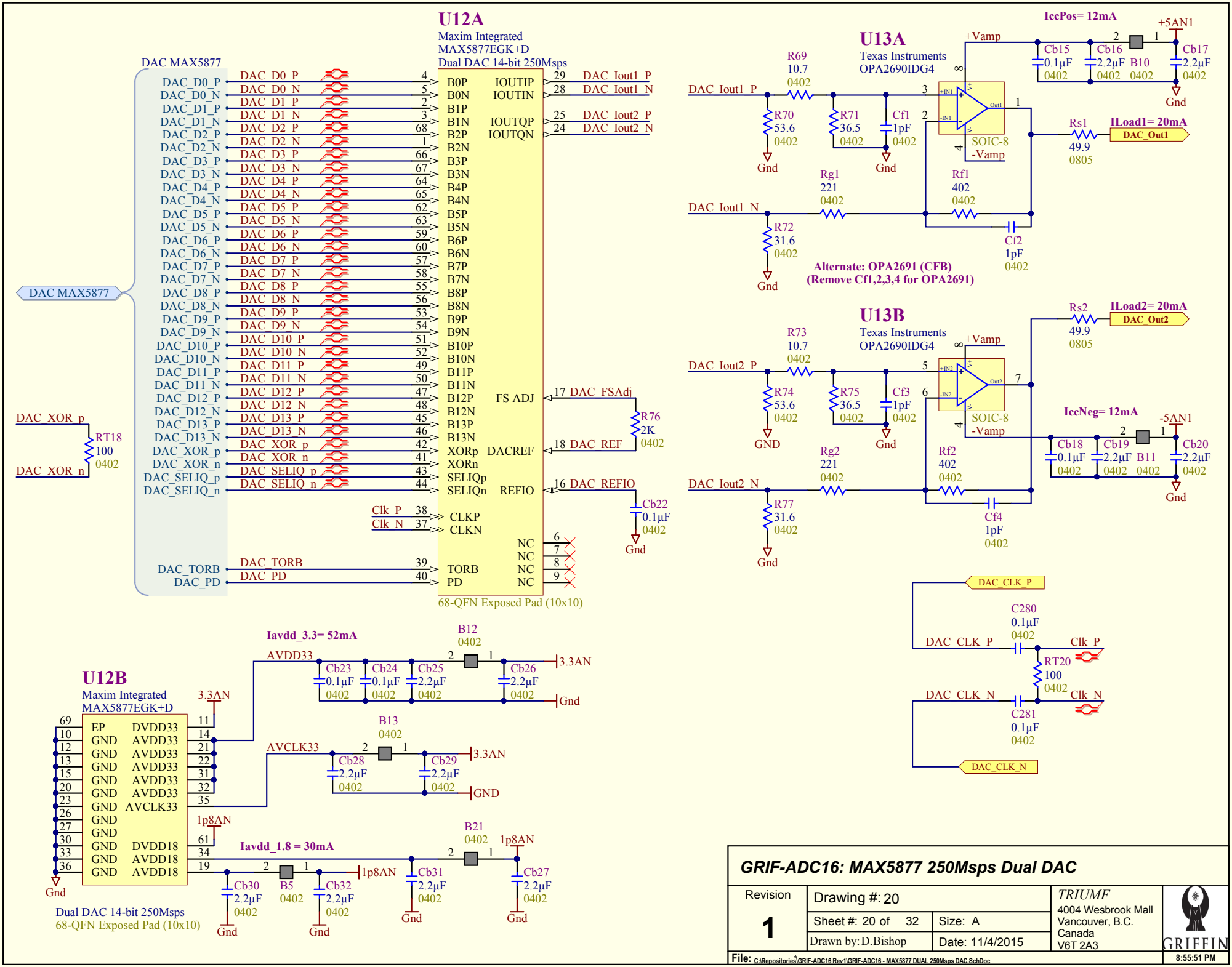
U12A
Maxim Integrated
MAX5877EGK+D
Dual DAC 14-bit 250Msps
DAC MAX5877
DAC_D0_P
DAC_D0_N
DAC_D1_P
DAC_D1_N
DAC_D2_P
DAC_D2_N
DAC_D3_P
DAC_D3_N
DAC_D4_P
DAC_D4_N
DAC_D5_P
DAC_D5_N
DAC_D6_P
DAC_D6_N
DAC_D7_P
DAC_D7_N
DAC_D8_P
DAC_D8_N
DAC_D9_P
DAC_D9_N
DAC_D10_P
DAC_D10_N
DAC_D11_P
DAC_D11_N
DAC_D12_P
DAC_D12_N
DAC_D13_P
DAC_D13_N
DAC_XOR_p
DAC_XOR_n
DAC_SELIQ_p
DAC_SELIQ_n
B0P
B0N
B1P
B1N
B2P
B2N
B3P
B3N
B4P
B4N
B5P
B5N
B6P
B6N
B7P
B7N
B8P
B8N
B9P
B9N
B10P
B10N
B11P
B11N
B12P
B12N
B13P
B13N
XORp
XORn
SELIQp
SELIQn
IOUTIP
IOUTIN
IOUTQP
IOUTQN
FS ADJ
DACREF
REFIO
CLKP
CLKN
TORB
PD
NC
DAC_Iout1_P
DAC_Iout1_N
DAC_Iout2_P
DAC_Iout2_N
DAC_FSAdj
DAC_REF
DAC_REFIO
Clk_P
Clk_N
DAC_TORB
DAC_PD
68-QFN Exposed Pad (10x10)
R76
2K
0402
Cb22
0.1µF
0402
Gnd
RT18
100
0402
U13A
Texas Instruments
OPA2690IDG4
IccPos= 12mA
+5AN1
+Vamp
-Vamp
SOIC-8
R69
10.7
0402
R70
53.6
0402
R71
36.5
0402
Cf1
1pF
0402
Rg1
221
0402
Rf1
402
0402
R72
31.6
0402
Cf2
1pF
0402
Cb15
0.1µF
0402
Cb16
2.2µF
0402
B10
0402
Cb17
2.2µF
0402
Rs1
49.9
0805
ILoad1= 20mA
DAC_Out1
Alternate: OPA2691 (CFB)
(Remove Cf1,2,3,4 for OPA2691)
U13B
Texas Instruments
OPA2690IDG4
R73
10.7
0402
R74
53.6
0402
R75
36.5
0402
Cf3
1pF
0402
Rg2
221
0402
Rf2
402
0402
R77
31.6
0402
Cf4
1pF
0402
Rs2
49.9
0805
ILoad2= 20mA
DAC_Out2
IccNeg= 12mA
-5AN1
Cb18
0.1µF
0402
Cb19
2.2µF
0402
B11
0402
Cb20
2.2µF
0402
U12B
Maxim Integrated
MAX5877EGK+D
Dual DAC 14-bit 250Msps
68-QFN Exposed Pad (10x10)
Iavdd_3.3= 52mA
3.3AN
AVDD33
AVCLK33
B12
0402
B13
0402
Cb23
0.1µF
0402
Cb24
0.1µF
0402
Cb25
2.2µF
0402
Cb26
2.2µF
0402
Cb28
2.2µF
0402
Cb29
2.2µF
0402
GND
Iavdd_1.8 = 30mA
1p8AN
B21
0402
B5
0402
Cb30
2.2µF
0402
Cb31
2.2µF
0402
Cb32
2.2µF
0402
Cb27
2.2µF
0402
DAC_CLK_P
DAC_CLK_N
C280
0.1µF
0402
C281
0.1µF
0402
RT20
100
0402
Clk_P
Clk_N
GRIF-ADC16: MAX5877 250Msps Dual DAC
Revision
1
Drawing #: 20
Sheet #: 20 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - MAX5877 DUAL 250Msps DAC.SchDoc
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GRIF - ADC16 - LTC2655 Quad Amplifier Offset DAC

Revision 1	Drawing #: 21		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 21 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - Quad DAC.SchDoc

8:55:51 PM

GRIF - ADC16 - LTC2655 Quad Amplifier Offset DAC

Revision 1	Drawing #: 21		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 21 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - Quad DAC.SchDoc

8:55:51 PM

GRIF - ADC16 - LTC2655 Quad Amplifier Offset DAC

Revision 1	Drawing #: 21		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 21 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - Quad DAC.SchDoc

8:55:51 PM

GRIF - ADC16 - LTC2655 Quad Amplifier Offset DAC

Revision 1	Drawing #: 21		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 21 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - Quad DAC.SchDoc

8:55:51 PM

MPM (Divider)

Vishay Dale Thin Film

, Surface Mount Divider Network

FEATURES

- Excellent long term ratio stability (ΔR ± 0.015 %, 2000 h, + 70 °C)
- Ratio tolerances to ± 0.01 %
- Low TCR tracking ± 2 ppm
- Standard JEDEC TO-236 package variation AB
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free RoHS* Available HALOGEN FREE

+5AN1
B1
350 mOhm Max
1 kOhm @ 100MHz
0603
C1 10µF 0603
C2 0.1µF 0603
GND
Ref+V
REF
+Vin
SHDN
GND
GND
Vout_F
Vout_S
GND
GND
Linear Technology
LTC6655BHMS8-3#PBF
8-MSOP
2ppm/°C
C3 10µF 0603
GND
3.0VRef
Rdiv
Vishay Thin Film
1K, 2K
±2ppm/°C Tracking
SOT-23
2K R2
1K R1
GND
1Vref
C4 0.1uF 0603
GND
C5 0.1µF 0603
Ref+V
GND
U1
LTC6240CS5#TRMPBF
TSOT-23-5
V+
V-
GND
R3 1R 0603
C6 10µF 0603
GND
ADC_Vref
C346 10nF 0603
R129 2.2K 0603

Total ADC reference load = (7K/4) = 1.75K
ADC ref current = 1/1.75K = 571uA

GRIF - ADC16 - ADC External Reference

Revision	Drawing #: 22		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
1	Sheet #: 22 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - ADC Volatge Reference.SchDoc

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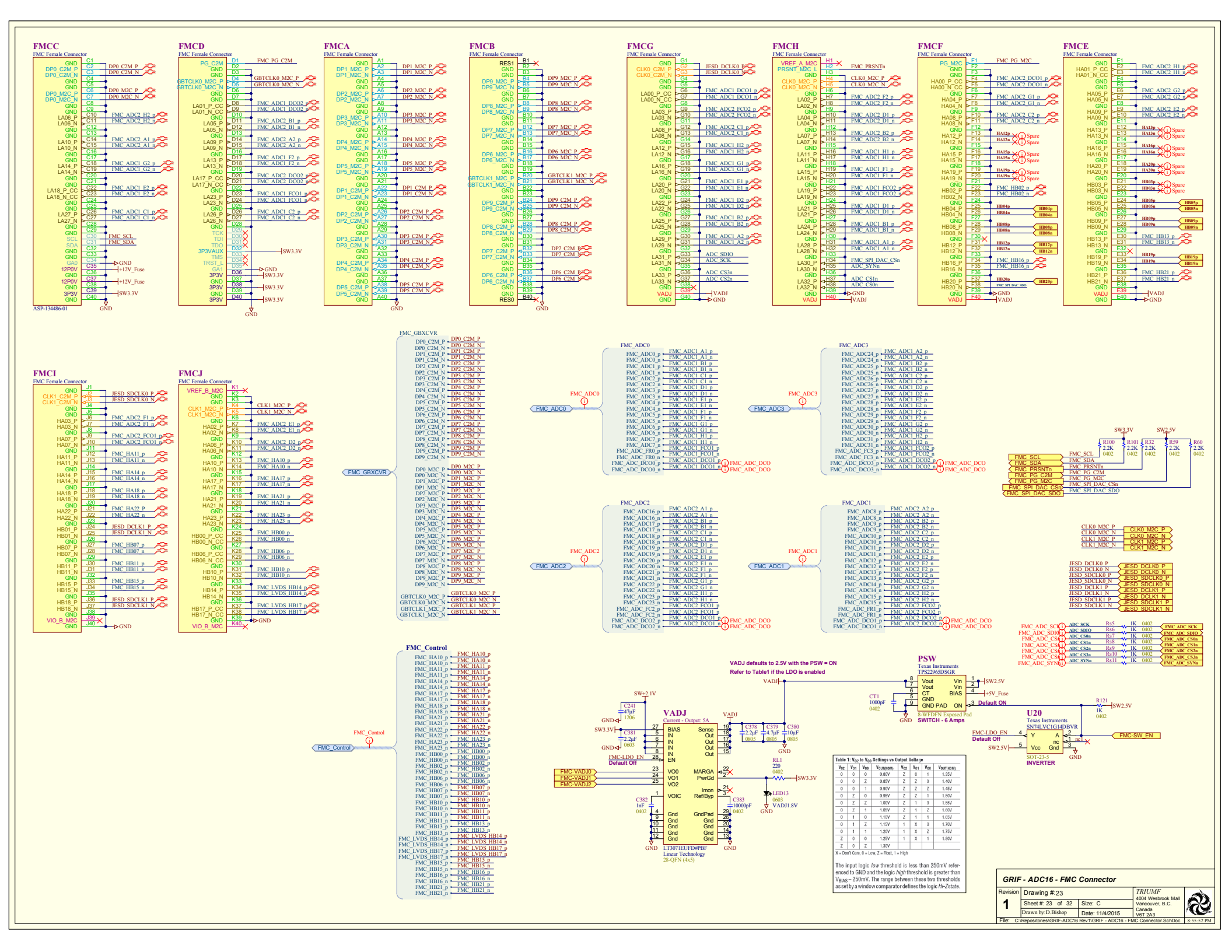
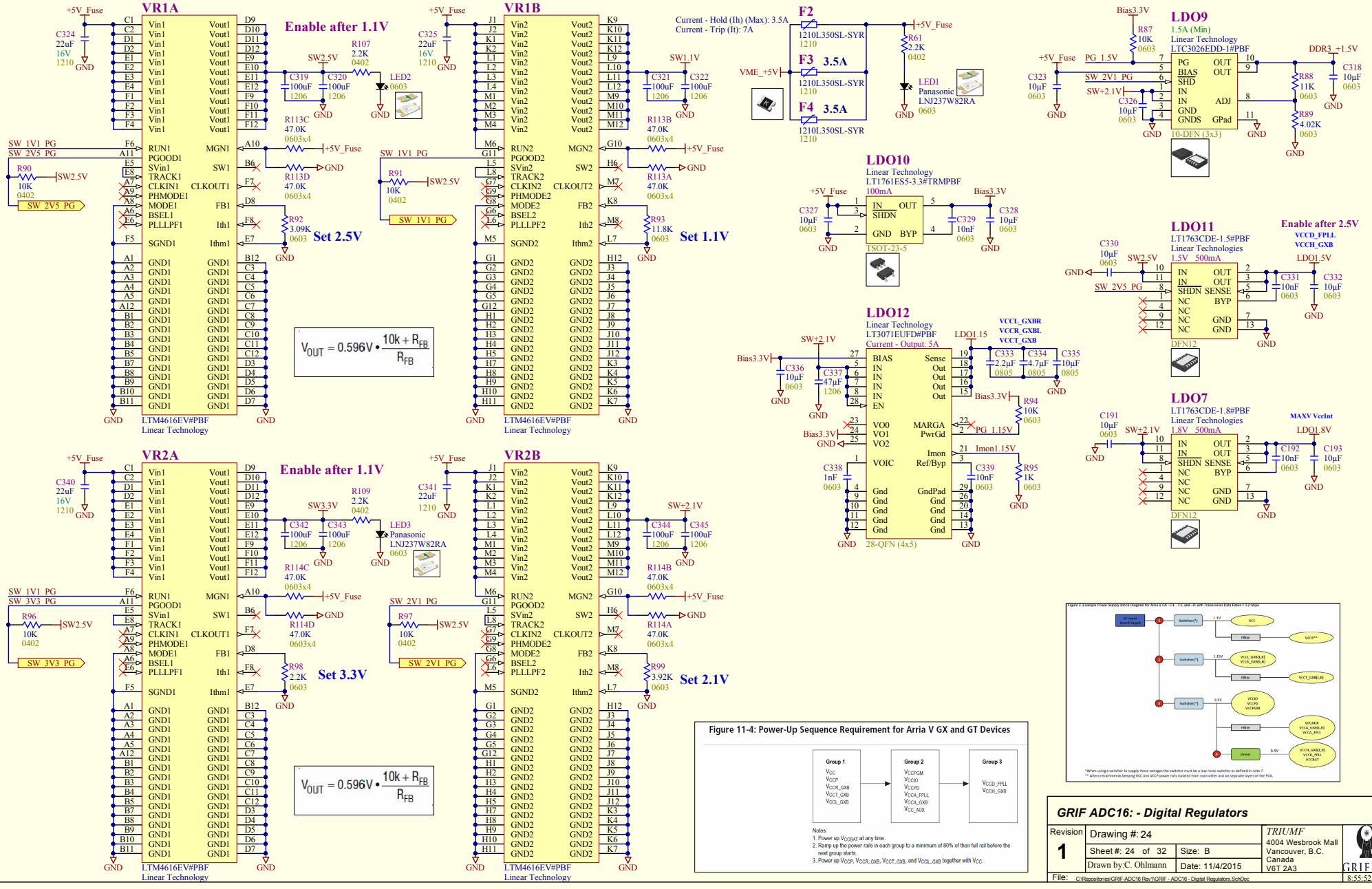

FMCC
FMC Female Connector
ASP-134486-01
FMCD
FMC Female Connector
FMCA
FMC Female Connector
FMCB
FMC Female Connector
FMCG
FMC Female Connector
FMCH
FMC Female Connector
FMCF
FMC Female Connector
FMCE
FMC Female Connector
FMCI
FMC Female Connector
FMCJ
FMC Female Connector
FMC_GBXCVR
FMC_ADC0
FMC_ADC3
FMC_ADC2
FMC_ADC1
FMC_Control
VADJ
Current - Output: 5A
LT3071EUFD#PBF
Linear Technology
28-QFN (4x5)
PSW
Texas Instruments
TPS22965DSGR
8-WFDFN Exposed Pad
SWITCH - 6 Amps
VADJ defaults to 2.5V with the PSW = ON
Refer to Table1 if the LDO is enabled
U20
Texas Instruments
SN74LVC1G14DBVR
SOT-23-5
INVERTER
Table 1: VCC to VOS Settings vs Output Voltage
The input logic low threshold is less than 250mV referenced to GND and the logic high threshold is greater than VBIAS − 250mV. The range between these two thresholds as set by a window comparator defines the logic Hi-Z state.
GRIF - ADC16 - FMC Connector
Revision 1
Drawing #:23
Sheet #: 23 of 32
Size: C
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - FMC Connector.SchDoc
8:55:52 PM


VR1A
Enable after 1.1V
Set 2.5V
VR1B
Set 1.1V
VR2A
Enable after 1.1V
Set 3.3V
VR2B
Set 2.1V
LTM4616EV#PBF
Linear Technology
F2
F3 3.5A
F4 3.5A
1210L350SL-SYR
LED1
Panasonic
LNJ237W82RA
LED2
LED3
LDO9
1.5A (Min)
Linear Technology
LTC3026EDD-1#PBF
10-DFN (3x3)
LDO10
Linear Technology
LT1761ES5-3.3#TRMPBF
100mA
TSOT-23-5
LDO11
LT1763CDE-1.5#PBF
Linear Technologies
1.5V 500mA
DFN12
Enable after 2.5V
LDO12
Linear Technology
LT3071EUFD#PBF
Current - Output: 5A
28-QFN (4x5)
LDO7
LT1763CDE-1.8#PBF
Linear Technologies
1.8V 500mA
MAXV VccInt
Figure 11-4: Power-Up Sequence Requirement for Arria V GX and GT Devices
GRIF ADC16: - Digital Regulators
TRIUMF
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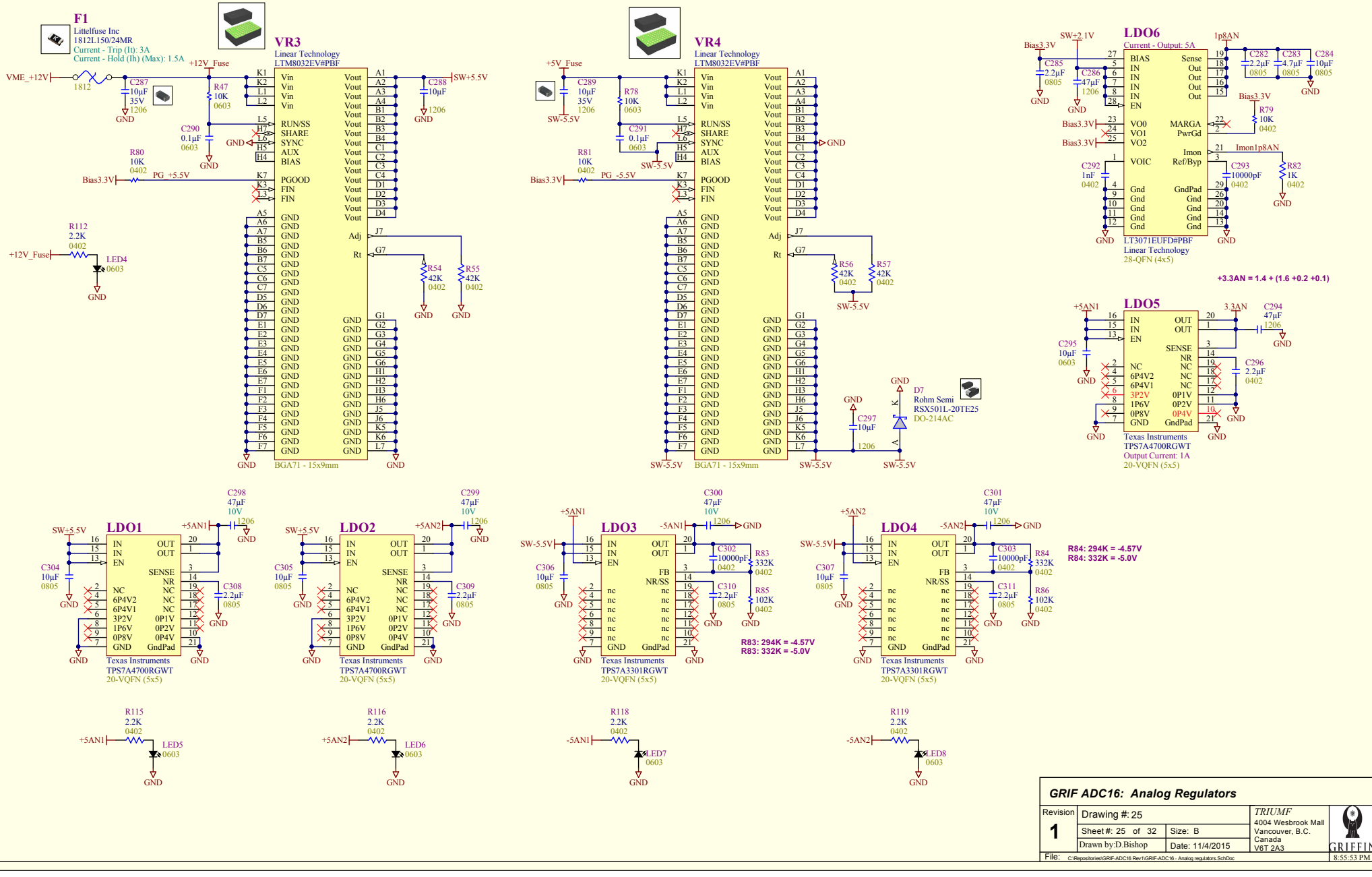
Canada
V6T 2A3
GRIFFIN


F1
Littelfuse Inc
1812L150/24MR
Current - Trip (It): 3A
Current - Hold (Ih) (Max): 1.5A
VME_+12V
1812
+12V_Fuse
C287 10µF 35V 1206
R47 10K 0603
C290 0.1µF 0603
R80 10K 0402
PG_+5.5V
Bias3.3V
VR3
Linear Technology
LTM8032EV#PBF
Vin
RUN/SS
SHARE
SYNC
AUX
BIAS
PGOOD
FIN
Vout
GND
Adj
Rt
BGA71 - 15x9mm
C288 10µF 1206
SW+5.5V
R54 42K 0402
R55 42K 0402
R112 2.2K 0402
LED4 0603
+5V_Fuse
C289 10µF 35V 1206
R78 10K 0603
C291 0.1µF 0603
R81 10K 0402
PG_-5.5V
SW-5.5V
VR4
Linear Technology
LTM8032EV#PBF
R56 42K 0402
R57 42K 0402
D7
Rohm Semi
RSX501L-20TE25
DO-214AC
C297 10µF 1206
LDO6
Current - Output: 5A
SW+2.1V
1p8AN
C285 2.2µF 0805
C286 47µF 1206
C282 2.2µF 0805
C283 4.7µF 0805
C284 10µF 0805
R79 10K 0402
Imon1p8AN
C292 1nF 0402
C293 10000pF 0402
R82 1K 0402
BIAS
IN
EN
VO0
VO1
VO2
VOIC
Sense
Out
MARGA
PwrGd
Imon
Ref/Byp
Gnd
GndPad
LT3071EUFD#PBF
Linear Technology
28-QFN (4x5)
+3.3AN = 1.4 + (1.6 +0.2 +0.1)
LDO5
+5AN1
3.3AN
C294 47µF 1206
C295 10µF 0603
C296 2.2µF 0402
NC
6P4V2
6P4V1
3P2V
1P6V
0P8V
SENSE
NR
FB
0P1V
0P2V
0P4V
Texas Instruments
TPS7A4700RGWT
Output Current: 1A
20-VQFN (5x5)
LDO1
SW+5.5V
+5AN1
C298 47µF 10V 1206
C304 10µF 0805
C308 2.2µF 0805
LDO2
+5AN2
C299 47µF 10V 1206
C305 10µF 0805
C309 2.2µF 0805
Texas Instruments
TPS7A4700RGWT
20-VQFN (5x5)
LDO3
-5AN1
C300 47µF 10V 1206
C306 10µF 0805
C302 10000pF 0402
R83 332K 0402
C310 2.2µF 0805
R85 102K 0402
R83: 294K = -4.57V
R83: 332K = -5.0V
Texas Instruments
TPS7A3301RGWT
20-VQFN (5x5)
LDO4
-5AN2
C301 47µF 10V 1206
C307 10µF 0805
C303 10000pF 0402
R84 332K 0402
C311 2.2µF 0805
R86 102K 0402
R84: 294K = -4.57V
R84: 332K = -5.0V
Texas Instruments
TPS7A3301RGWT
20-VQFN (5x5)
R115 2.2K 0402
LED5 0603
R116 2.2K 0402
LED6 0603
R118 2.2K 0402
LED7 0603
R119 2.2K 0402
LED8 0603
GRIF ADC16: Analog Regulators
Revision 1
Drawing #: 25
Sheet #: 25 of 32
Size: B
Drawn by:D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - Analog regulators.SchDoc
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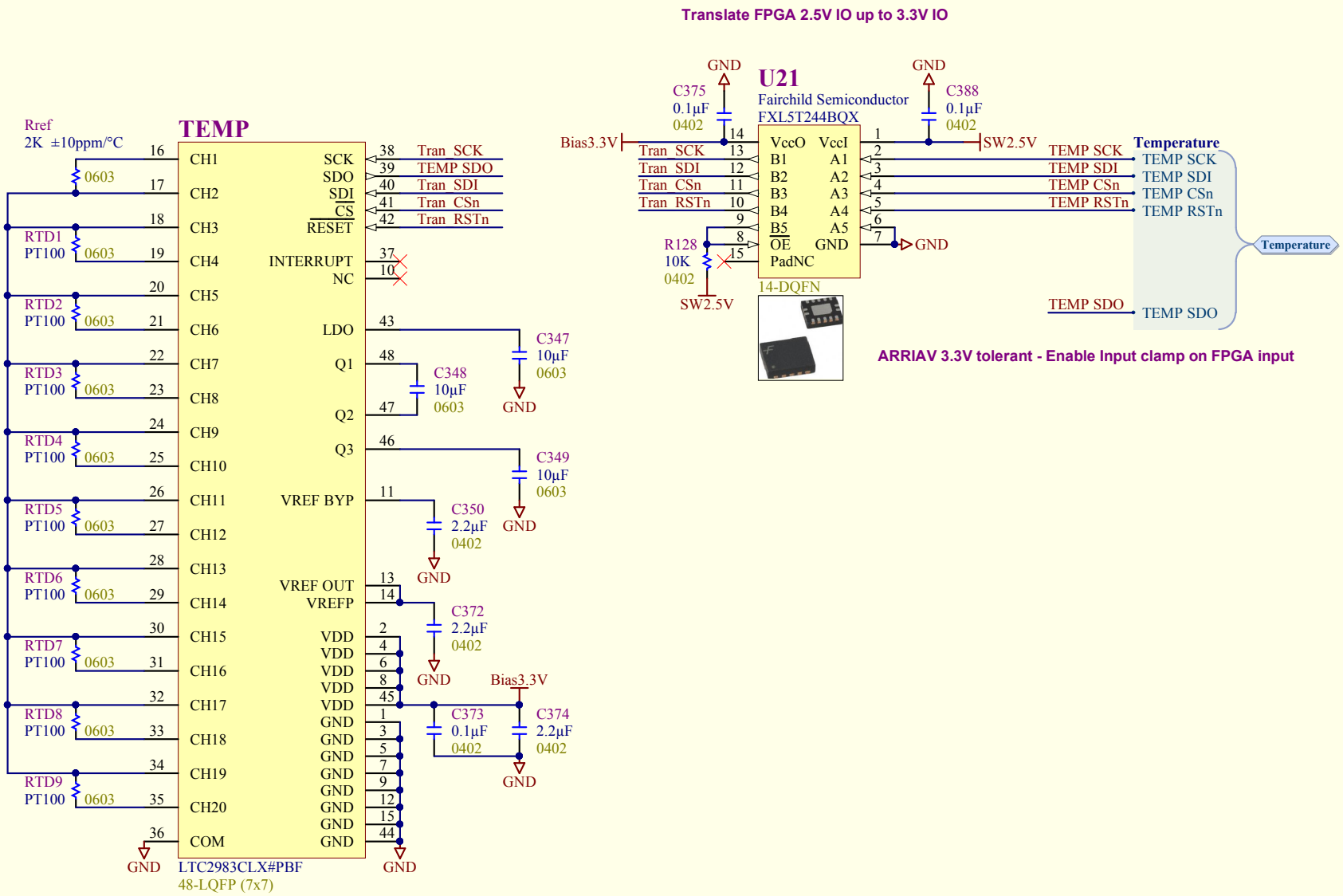
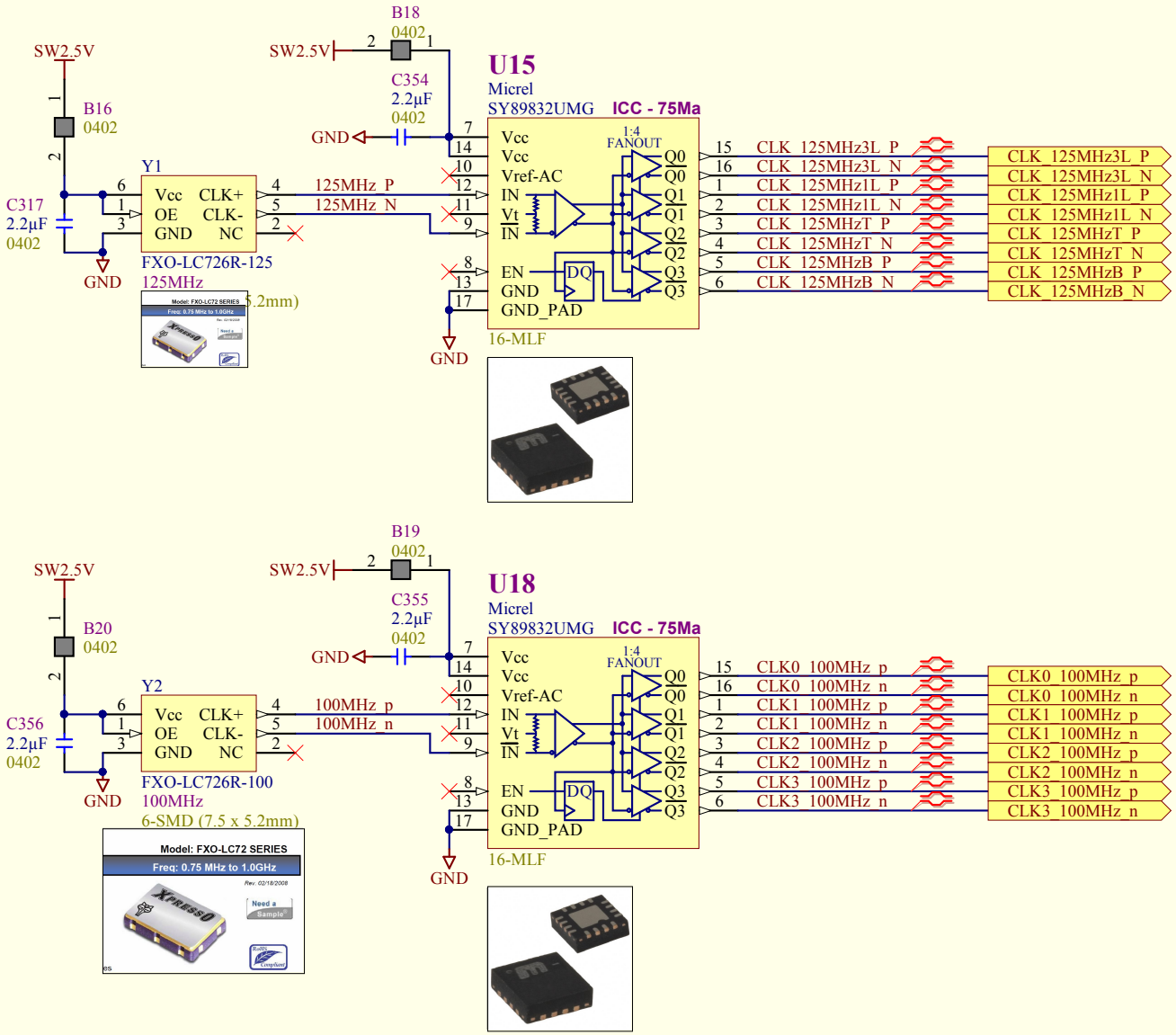

Translate FPGA 2.5V IO up to 3.3V IO
TEMP
Rref
2K ±10ppm/°C
LTC2983CLX#PBF
48-LQFP (7x7)
U21
Fairchild Semiconductor
FXL5T244BQX
14-DQFN
ARRIAV 3.3V tolerant - Enable Input clamp on FPGA input
Temperature
GRIF - ADC16 - Temperature Sensors
Revision
1
Drawing #: 26
Sheet #: 26 of 32
Size: A
Drawn by: D.Bishop
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - Temperature Sensors.SchDoc
8:55:53 PM



GRIF-ADC16: Clock Distribution

Revision	Drawing #: 27		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
1	Sheet #: 27 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - Clock Distribution.SchDoc

GRIFFIN

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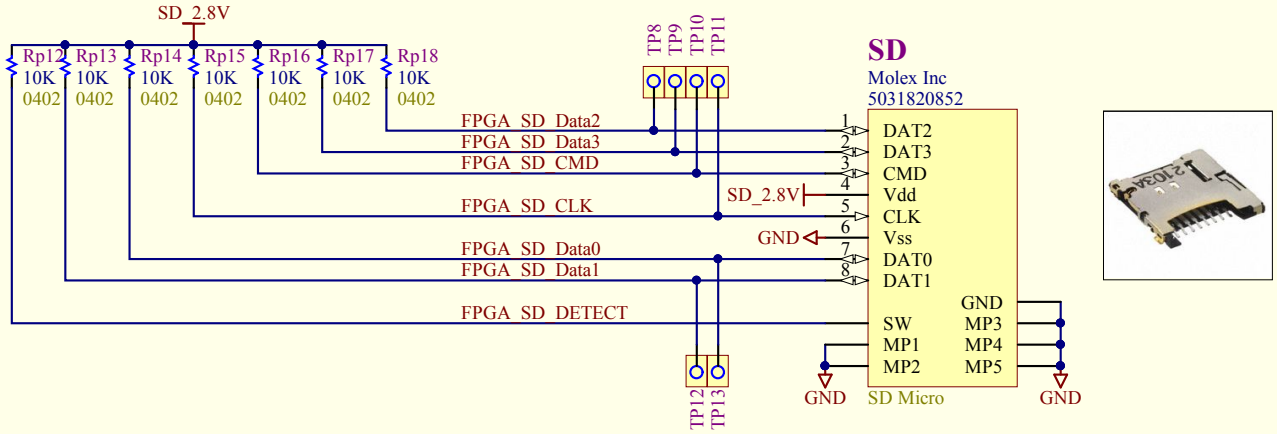
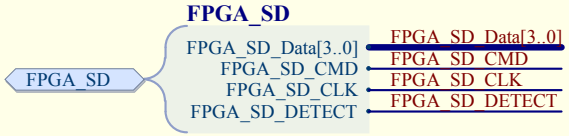
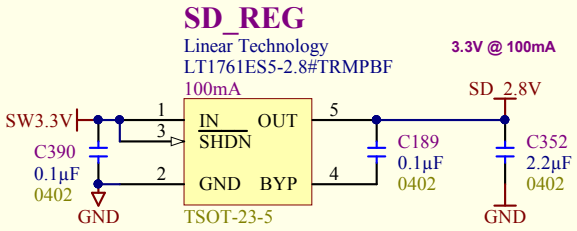
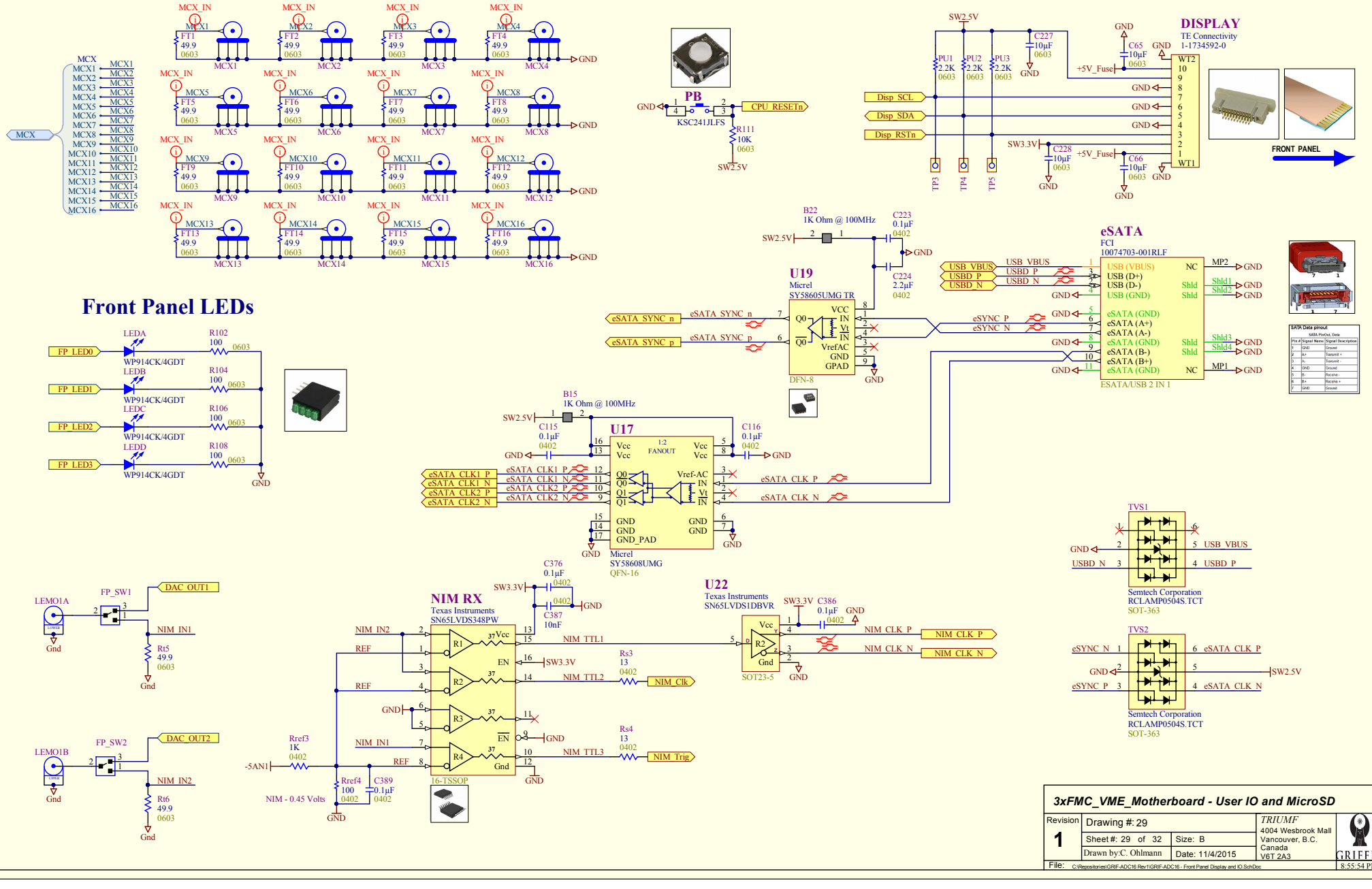
MicroSD Memory Interface







GRIF - ADC16: MicroSD				
Revision 1	Drawing #: 28		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	GRIFFIN
	Sheet #: 28 of 32	Size: A		
	Drawn by: C. Ohlmann	Date: 11/4/2015		
File: C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - MicroSD.SchDoc				8:55:53 PM


MCX
MCX_IN
GND
PB
KSC241JLFS
CPU_RESETn
R111
10K
0603
SW2.5V
DISPLAY
TE Connectivity
1-1734592-0
Disp_SCL
Disp_SDA
Disp_RSTn
SW3.3V
+5V_Fuse
WT1
WT2
FRONT PANEL
TP3
TP4
TP5
Front Panel LEDs
FP_LED0
FP_LED1
FP_LED2
FP_LED3
LEDA
LEDB
LEDC
LEDD
R102
R104
R106
R108
100
0603
WP914CK/4GDT
U19
Micrel
SY58605UMG TR
DFN-8
B22
1K Ohm @ 100MHz
C223
0.1µF
0402
C224
2.2µF
0402
eSATA_SYNC_n
eSATA_SYNC_p
eSATA
FCI
10074703-001RLF
ESATA/USB 2 IN 1
USB_VBUS
USB_P
USB_N
eSYNC_P
eSYNC_N
B15
1K Ohm @ 100MHz
C115
C116
0.1µF
0402
U17
1:2
FANOUT
Micrel
SY58608UMG
QFN-16
eSATA_CLK1_P
eSATA_CLK1_N
eSATA_CLK2_P
eSATA_CLK2_N
eSATA_CLK_P
eSATA_CLK_N
TVS1
TVS2
Semtech Corporation
RCLAMP0504S.TCT
SOT-363
LEMO1A
LEMO1B
FP_SW1
FP_SW2
DAC_OUT1
DAC_OUT2
NIM_IN1
NIM_IN2
Rt5
Rt6
49.9
0603
NIM RX
Texas Instruments
SN65LVDS348PW
C376
0.1µF
C387
10nF
REF
EN
NIM_TTL1
NIM_TTL2
NIM_TTL3
Rs3
Rs4
13
0402
NIM_Clk
NIM_Trig
16-TSSOP
Rref3
1K
Rref4
100
C389
NIM - 0.45 Volts
-5AN1
U22
Texas Instruments
SN65LVDS1DBVR
C386
SOT23-5
NIM_CLK_P
NIM_CLK_N
3xFMC_VME_Motherboard - User IO and MicroSD
Revision
1
Drawing #: 29
Sheet #: 29 of 32
Size: B
Drawn by:C. Ohlmann
Date: 11/4/2015
TRIUMF
4004 Wesbrook Mall
Vancouver, B.C.
Canada
V6T 2A3
GRIFFIN
File:
C:\Repositories\GRIF-ADC16 Rev1\GRIF-ADC16 - Front Panel Display and IO.SchDoc
8:55:54 PM

VccR and VccT = 3.3V+/-5% (300mA max)

SW2.5V GND

RP11
MNR18E0APJ472
4.7k
0602x8

SFP CTL/STAT
SFP_TX_Fault
SFP_TX_Disable
SFP_SDA
SFP_SCL
SFP_ModDet
SFP_RateSelect
SFP_LOS
MAC_SCL
MAC_SDA

SFP

1	VeeT	VeeT	20
2	TX_Fault	TD-	19
3	TX_Disable	TD+	18
4	MODDEF2	VeeT	17
5	MODDEF1	VccT	16
6	MODDEF0	VccR	15
7	RateSelect	VeeR	14
8	LOS	RD+	13
9	VeeR	RD-	12
10	VeeR	VeeR	11

SFP_TX_N
SFP_TX_P
SFP_RX_P
SFP_RX_N
VccT
VccR

TP6 TP7

SFP Shield
1489669-1
TE Connectivity

SFP Connector
1367073-1
TE Connectivity

C357 10µF 0603
L5 1µH 0603
L6 1µH 0603
C358 10µF 0603
C359 0.1µF 0603
C360 0.1µF 0603
C361 10µF 0603
SW3.3V

MAC_ADD
Microchip Technology
24AA02E48T-I/OT
SOT23-5
I2C Address 0xA0

R126 2.2K 0402
R127 2.2K 0402
C384 0.1µF 0402

AFBR-57M5APZ
Digital Diagnostic SFP, 850 nm, 2.125/1.0625 and 1.25 GBd Ethernet, RoHS Compliant Optical Transceiver

Avago TECHNOLOGIES

Data Sheet

850 nm, SFP (Small Form Pluggable), RoHS Compliant, Low Voltage (3.3 V) Digital Diagnostic Optical Transceiver

Digital Diagnostic Interface and Serial Identification

The 2-wire serial interface is based on ATMEL AT24C01A series EEPROM protocol and signaling detail. Conventional EEPROM memory, bytes 0-255 at memory address 0xA0, is organized in compliance with SFF-8074i. New digital diagnostic information, bytes 0-255 at memory address 0xA2, is compliant to SFF-8472. The new diagnostic information provides the opportunity for Predictive Failure Identification, Compliance Prediction, Fault Isolation and Component Monitoring.

GRIF - ADC16 - SFP Link

Revision 1	Drawing #: 30		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 30 of 32	Size: A	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - SFP Link.SchDoc 8:55:54 PM

GRIFFIN

1Gb, 3V, Multiple I/O Serial NOR Flash Memory
Features

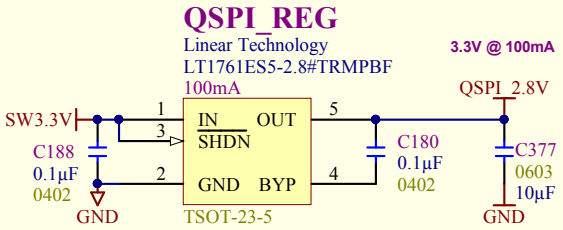
Micron Serial NOR Flash Memory

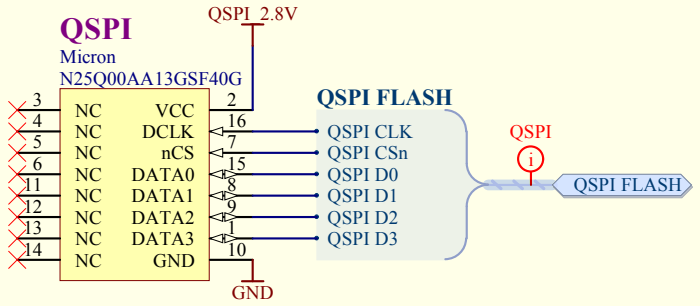
3V, Multiple I/O, 4KB Sector Erase

N25Q00AA

Features

- Stacked device (four 256Mb die)
- SPI-compatible serial bus interface
- Double transfer rate (DTR) mode
- 2.7–3.6V single supply voltage
- 108 MHz (MAX) clock frequency supported for all protocols in single transfer rate (STR) mode
- 54 MHz (MAX) clock frequency supported for all protocols in DTR mode
- Dual/quad I/O instruction provides increased throughput up to 54 MB/s
- Supported protocols
  - Extended SPI, dual I/O, and quad I/O
  - DTR mode supported on all
- Execute-in-place (XIP) mode for all three protocols
  - Configurable via volatile or nonvolatile registers
  - Enables memory to work in XIP mode directly after power-on
- PROGRAM/ERASE SUSPEND operations
- Available protocols
  - Available READ operations
  - Quad or dual output fast read
  - Quad or dual I/O fast read
- Flexible to fit application
  - Configurable number of dummy cycles
  - Output buffer configurable
- Software reset
- 3-byte and 4-byte addressability mode supported
- 64-byte, user-lockable, one-time programmable (OTP) dedicated area
- Erase capability
  - Subsector erase 4KB uniform granularity blocks
  - Sector erase 64KB uniform granularity blocks
  - Single die erase (32MB)
- Write protection
  - Software write protection applicable to every 64KB sector via volatile lock bit
  - Hardware write protection: protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and TB)
  - Additional smart protections, available upon request
- Electronic signature
  - JEDEC-standard 2-byte signature (BA21h)
  - Unique ID code (UID): 17 read-only bytes, including: Two additional extended device ID bytes to identify device factory options; and customized factory data (14 bytes)
- Minimum 100,000 ERASE cycles per sector
- More than 20 years data retention
- Packages – JEDEC-standard, all RoHS-compliant
  - L-PBGA-24b05/6mm x 8mm (also known as LBGA24)
  - SOP2-16/300 mils (also known as SO16W, SO16-Wide, SOIC-16)





16-SOIC (7.50mm Width)

GRIF - ADC16 - SPIx4 Micron Flash

Revision	Drawing #: 31		TRIUMF
1	Sheet #: 31 of 32	Size: A	4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - QSPI Memory.SchDoc

GRIFFIN

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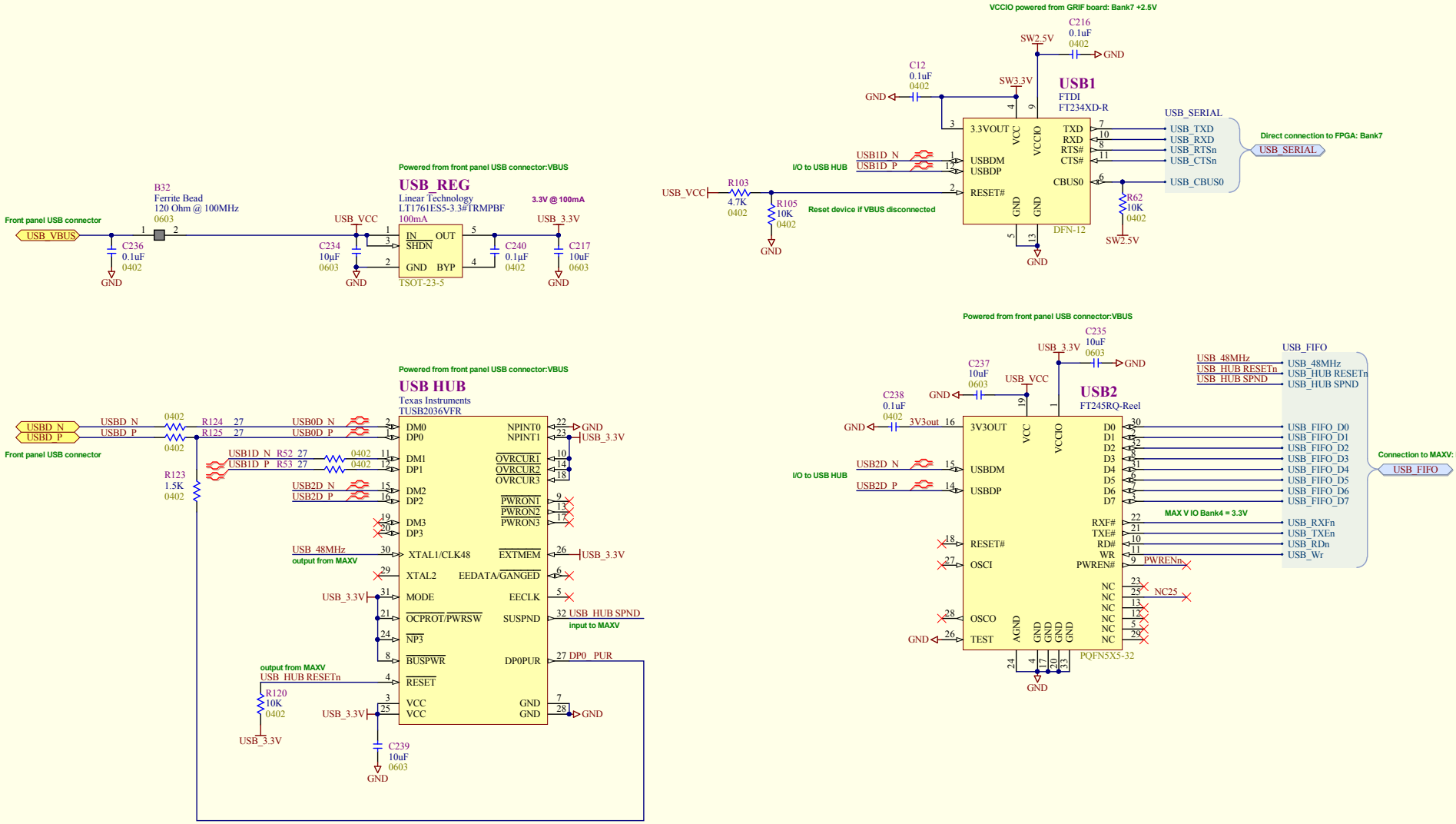
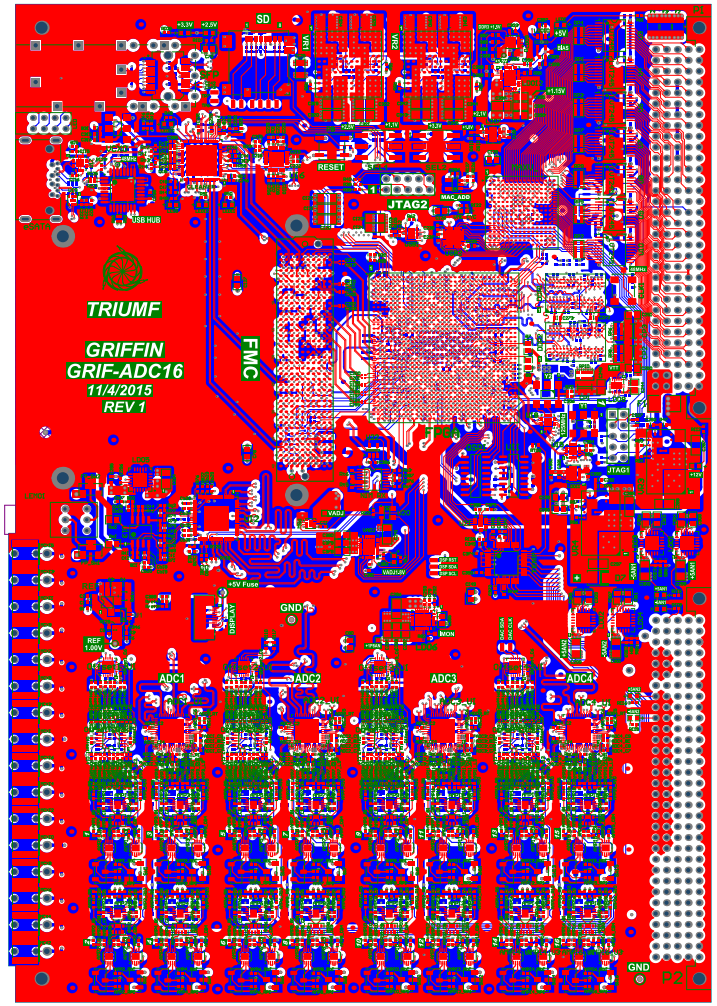


GRIF - ADC16 - USB FTDI Interfaces

Revision 1	Drawing #: 32		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
	Sheet #: 32 of 32	Size: B	
	Drawn by: D.Bishop	Date: 11/4/2015	

File: C:\Repositories\GRIF-ADC16 Rev1\GRIF - ADC16 - USB Interface.SchDoc — 8:55:54 PM

Cannot open file TRIUMF.BMP


TRIUMF
GRIFFIN
GRIF-ADC16
11/4/2015
REV 1
FMC
SD
RESET
JTAG2
JTAG1
USB HUB
ADC1
ADC2
ADC3
ADC4
GND
P2