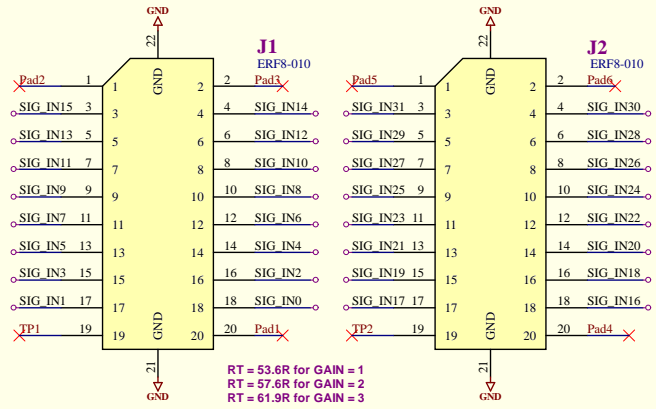
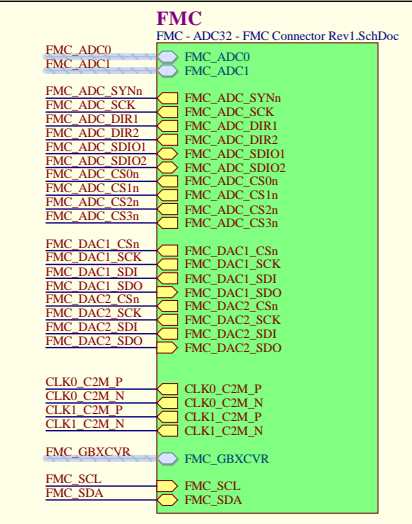
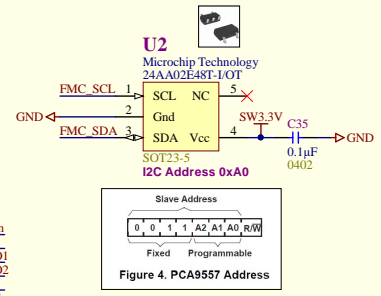
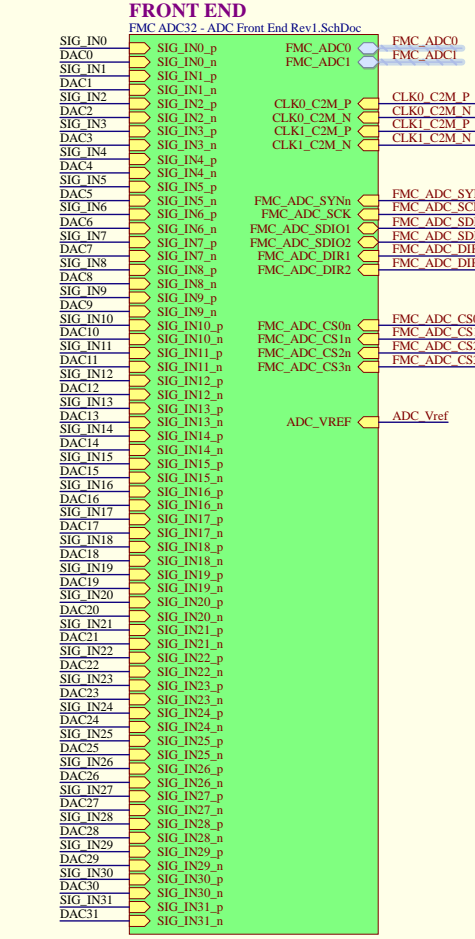
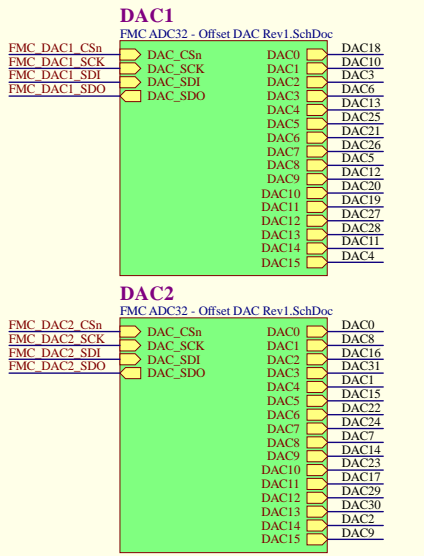


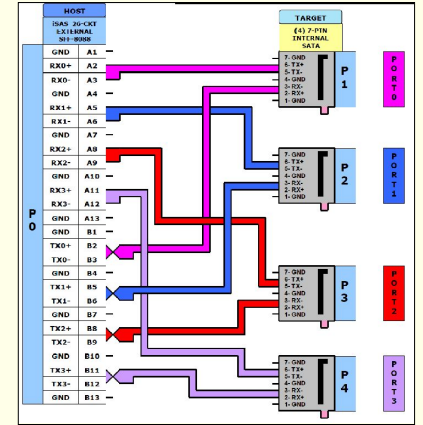
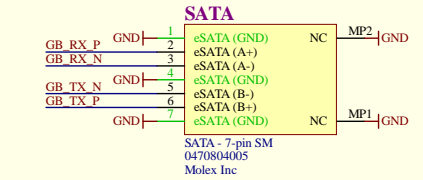
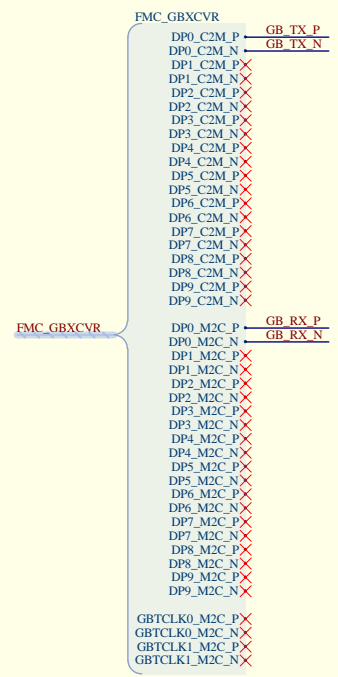
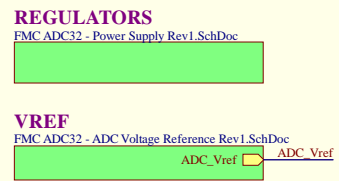
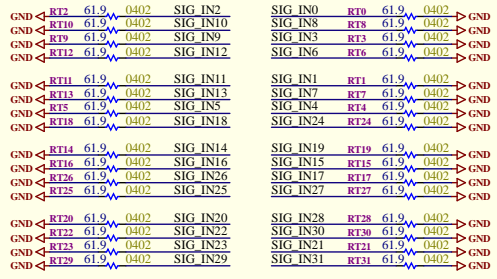


HeatSink  
HS1 HS4  
HS2 HS3  
GND GND

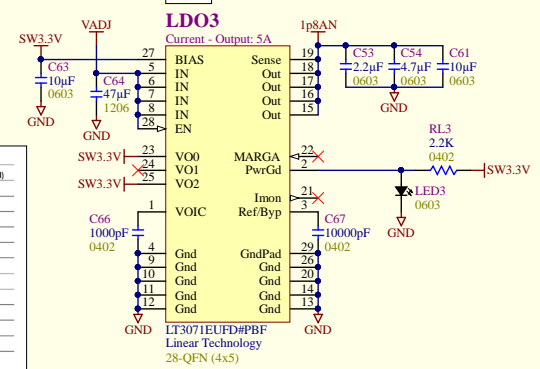
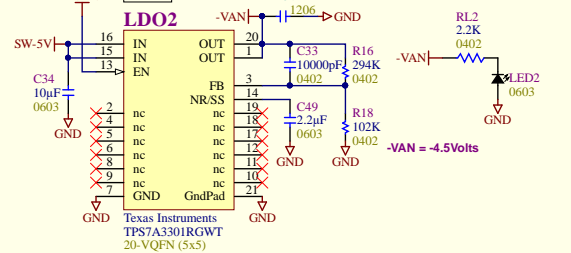
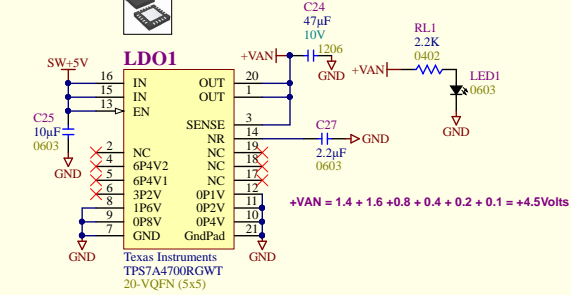
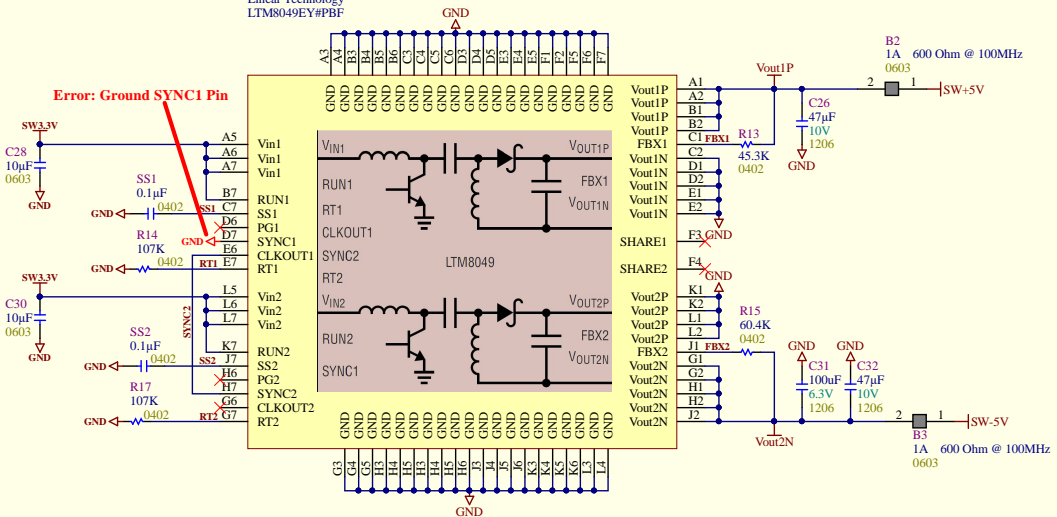
Advanced Thermal Solutions Inc.  
ATS-P1-39-C2-R0  
57.9X60.96X5.84(mm)



RT = 53.6R for GAIN = 1  
RT = 57.6R for GAIN = 2  
RT = 61.9R for GAIN = 3

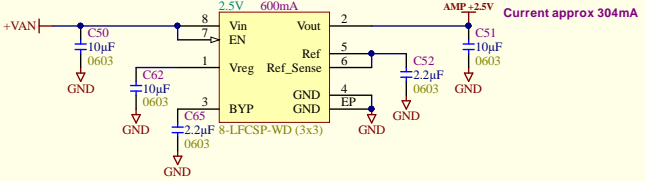


**VR1**  
Linear Technology  
LTM8049EY#PBF



**LDO4**

Analog Devices Inc.  
ADM7154ACFZ-2.5-R7  
2.5V 600mA



**LDO5**

Analog Devices Inc.  
ADP7185ACPZN2.5-R7  
-2.5V -500mA

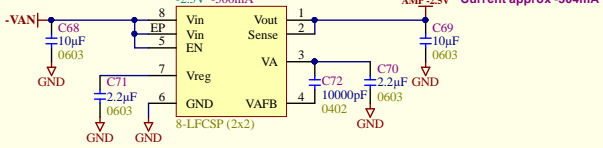


Table 1: V<sub>DD</sub> to V<sub>DD</sub> Settings vs Output Voltage

V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub> (nom)	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub> (nom)
0	0	0	0.80V	Z	0	1	1.35V
0	0	0	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	1	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High

The input logic *low* threshold is less than 250mV referenced to GND and the logic *high* threshold is greater than V<sub>BIAS</sub> - 250mV. The range between these two thresholds as set by a window comparator defines the logic *H-Z* state.

**FMC ADC32 - Power Regulators**

Revision	Drawing #: 2	TRIUMF
<b>1</b>	Sheet #: 2 of 8	4004 Wesbrook Mall
	Size: B	Vancouver, B.C.
	Drawn by: D.Bishop	Canada
	Date: 3/10/2018	V6T 2A3



# MPM (Divider)

Vishay Dale Thin Film

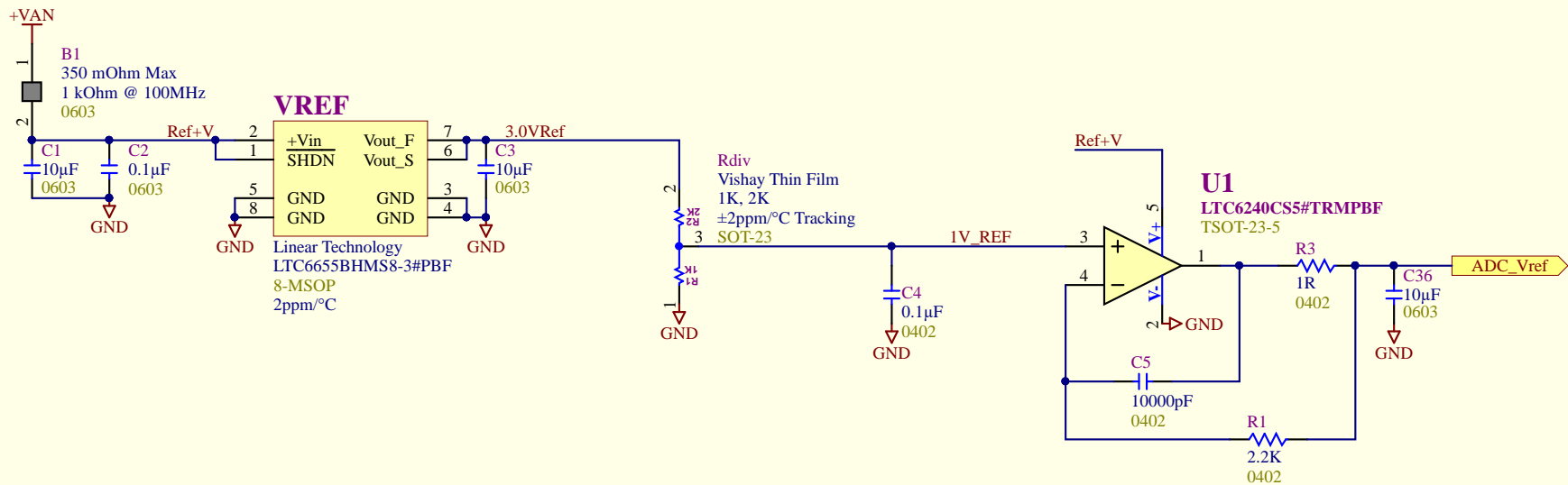
## Surface Mount Divider Network

### FEATURES

- Excellent long term ratio stability ( $\Delta R \pm 0.015\%$ , 2000 h, +70 °C)
- Ratio tolerances to  $\pm 0.01\%$
- Low TCR tracking  $\pm 2$  ppm
- Standard JEDEC TO-236 package variation AB
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

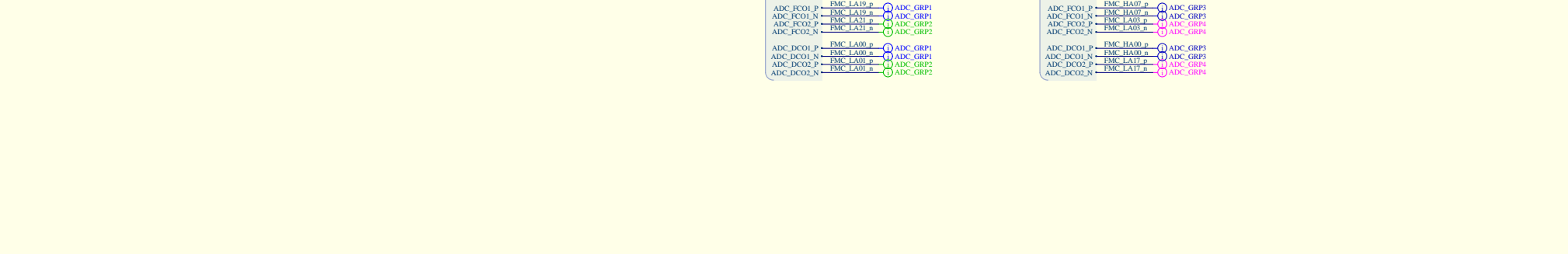
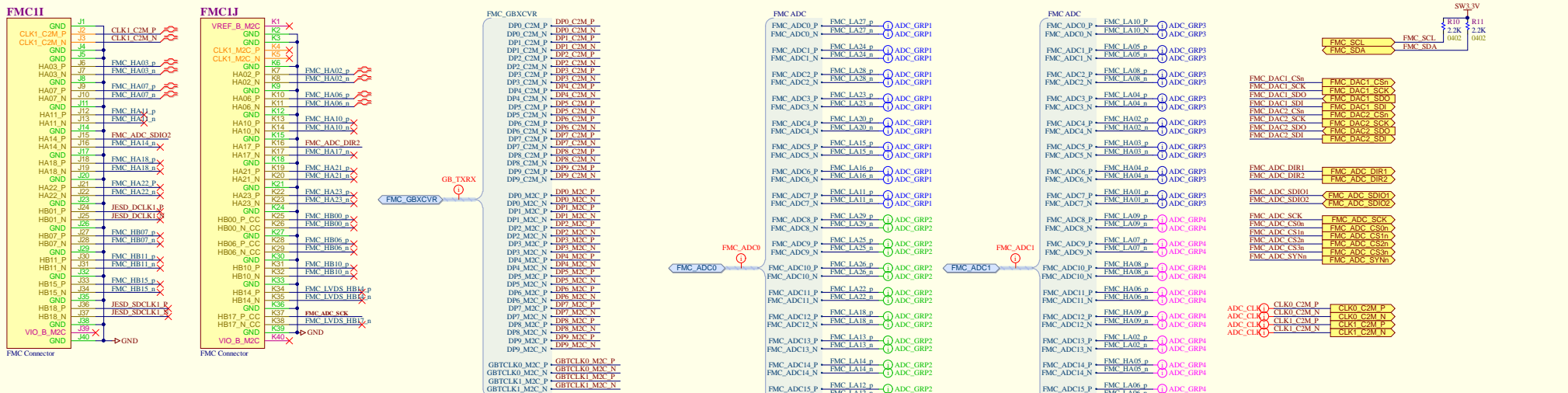
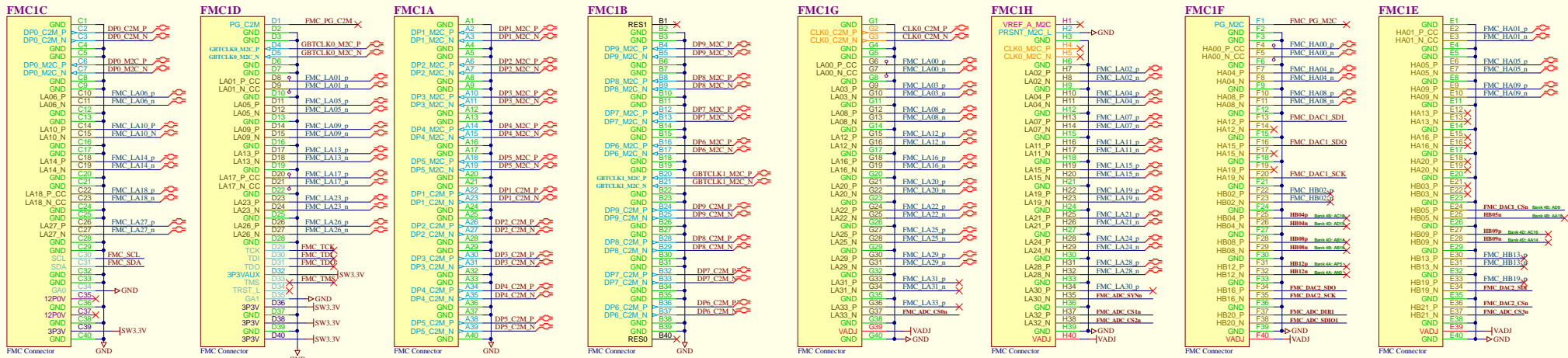


RoHS\*  
Available  
HALOGEN  
FREE



### FMC ADC32 - ADC Voltage Reference

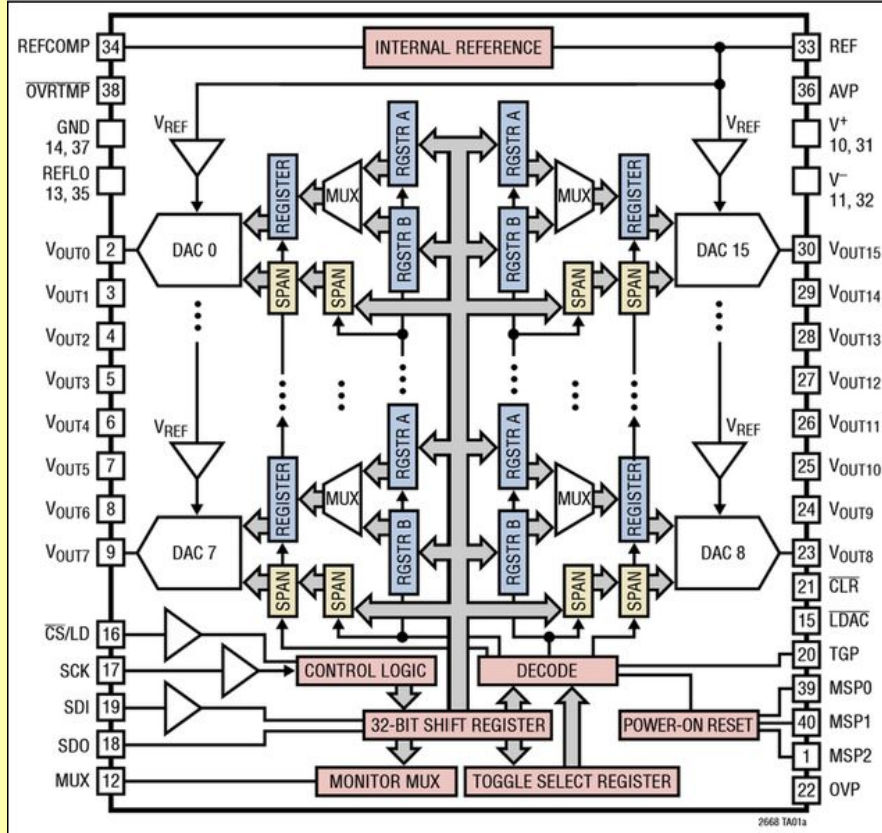
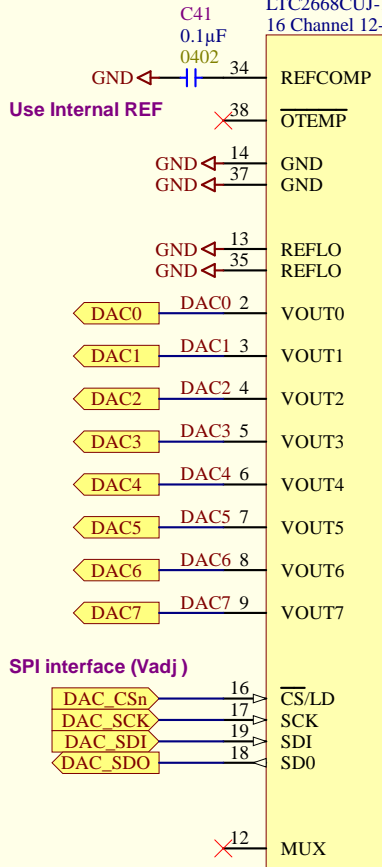
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	Sheet #: 3 of 8	Size: A		
	Drawn by: D.Bishop	Date: 3/10/2018		



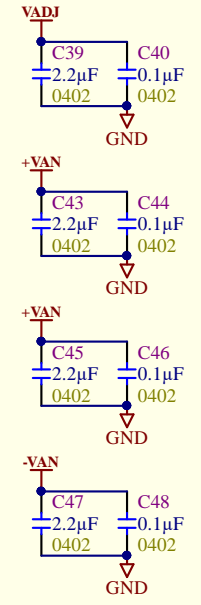
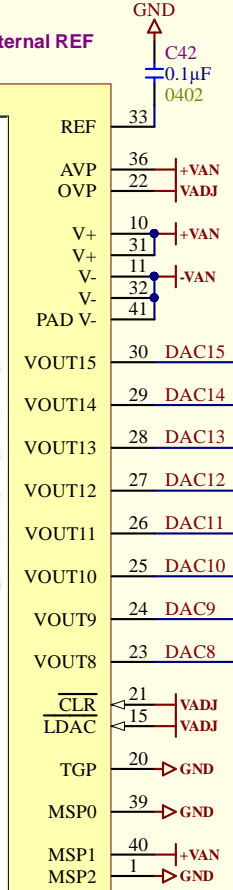


# DAC

Linear Technology  
LTC2668CUJ-12#PBF  
16 Channel 12-bit bipolar DAC



Use Internal REF



40-QFN (6x6)

DAC updates via SPI interface

Not using toggle operation

Manual Span +/- 2.5V Mid Scale

The device has a precision 2.5V integrated reference with a typical temperature drift of 2ppm/°C. To use the internal reference, the REFCOMP pin should be left floating (no DC path to ground). In addition, the RD bit in the config register must have a value of 0. This value is reset to 0 at power-up, or it can be reset using the *Config* command, 0111b. Figure 9 shows the command syntax.

### Manual Span Operation

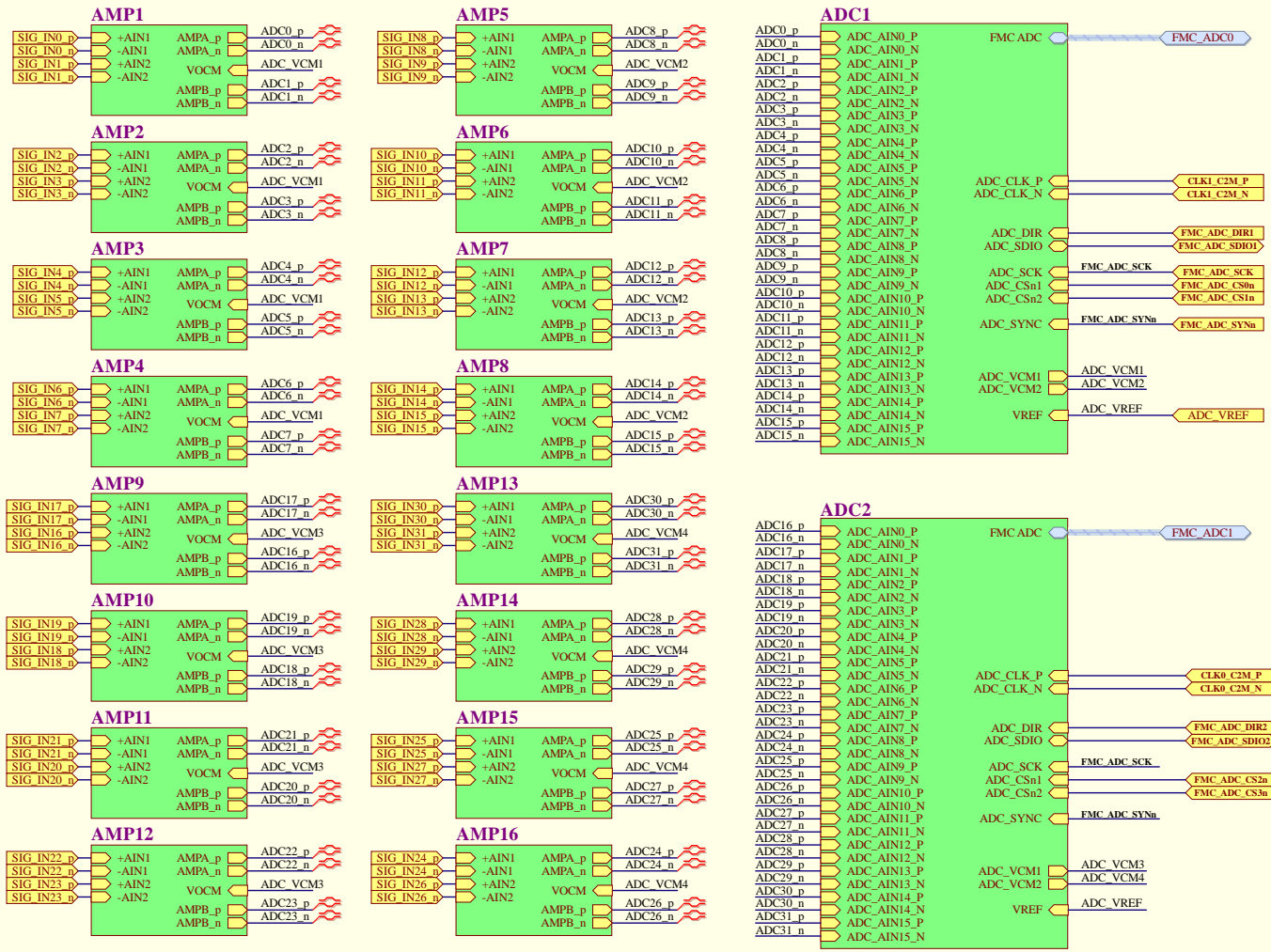
Multiple output ranges are not needed in all applications. By tying the MSPAN pins (MSP2, MSP1 and MSP0) to GND and/or AVP, any output range can be hardware-configured without additional operational overhead. Zero-scale and mid-scale reset options are also available for the unipolar modes (see Table 4).

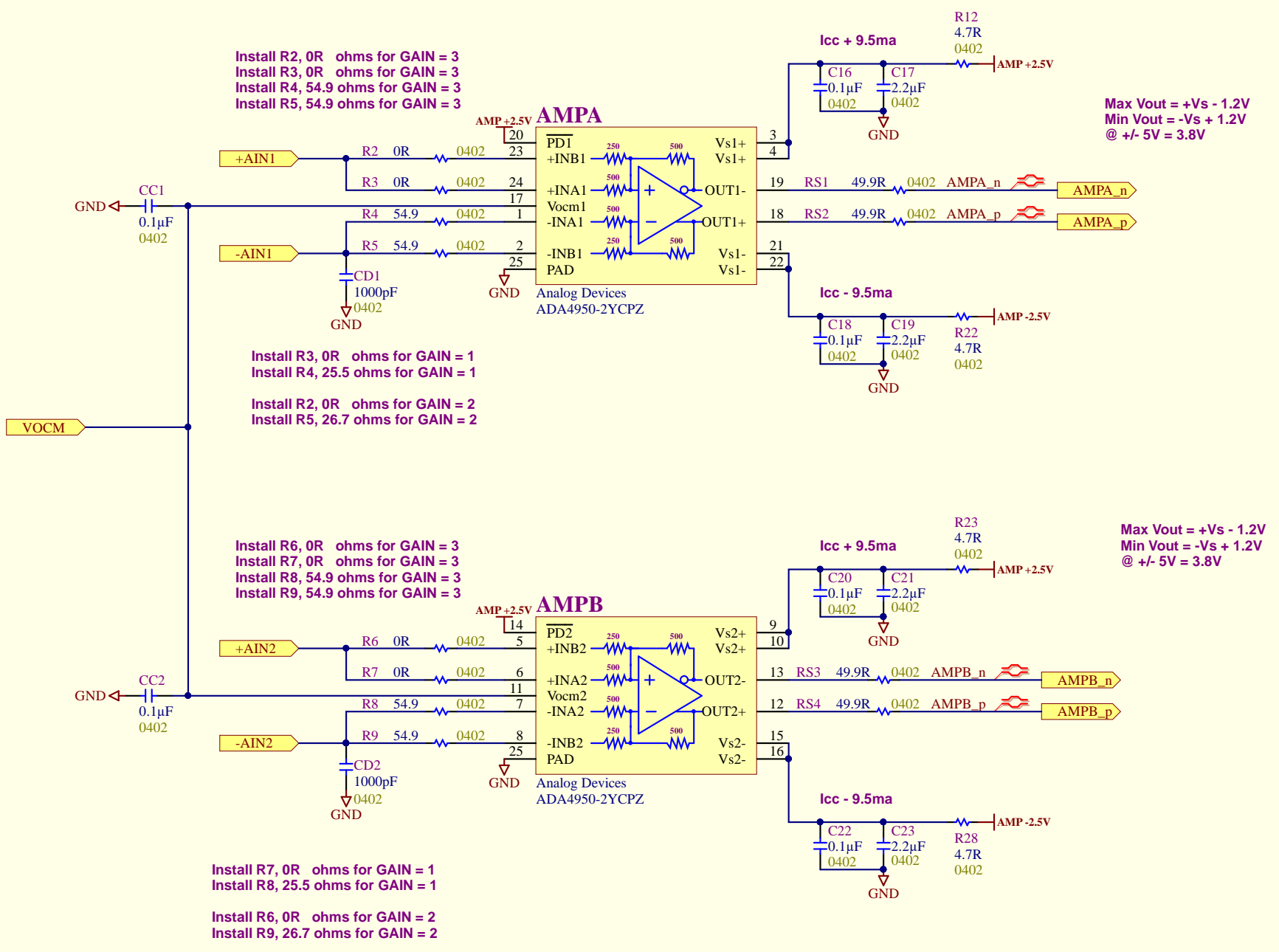
Table 4. MSPAN Pin Configurations

MSP2	MSP1	MSP0	OUTPUT RANGE	RESET CODE	MANUAL SPAN	SOFT-SPAN
0	0	0	±10V	Mid-Scale	X	
0	0	AVP	±5V	Mid-Scale	X	
0	AVP	0	±2.5V	Mid-Scale	X	
0	AVP	AVP	0V to 10V	Zero-Scale	X	
AVP	0	0	0V to 10V	Mid-Scale	X	
AVP	0	AVP	0V to 5V	Zero-Scale	X	
AVP	AVP	0	0V to 5V	Mid-Scale	X	
AVP	AVP	AVP	0V to 5V	Zero-Scale		X

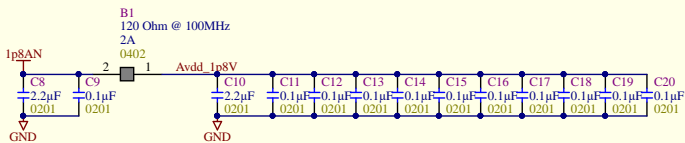
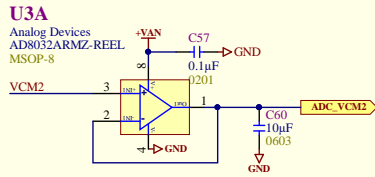
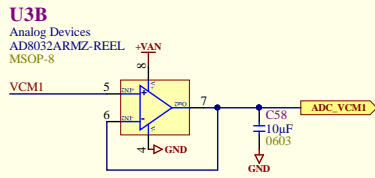
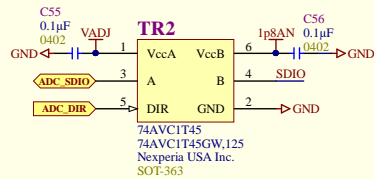
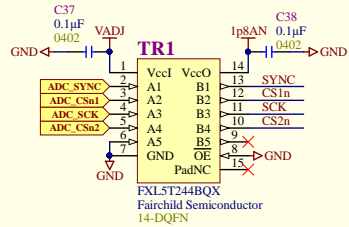
## FMC ADC32 - Offset DAC (LTC2668)

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	Drawn by: D.Bishop	Date: 3/10/2018		
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7:00:17 PM				

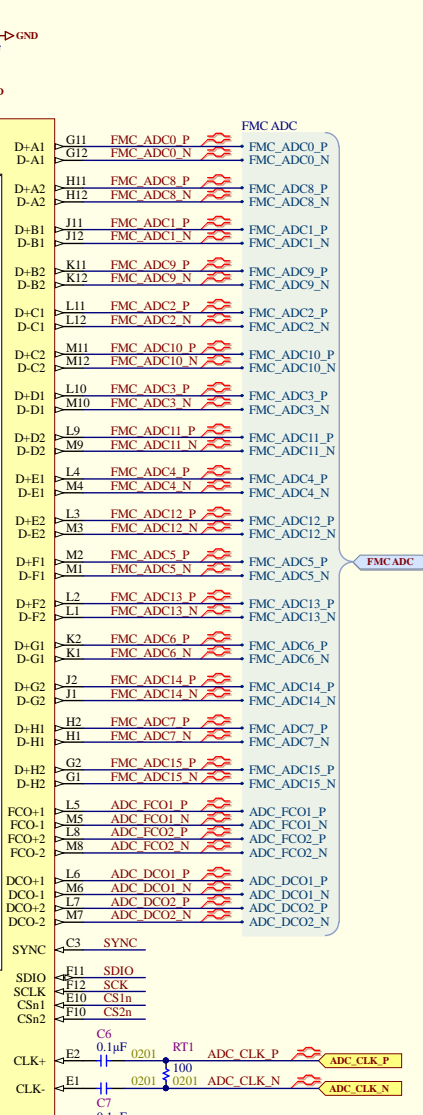
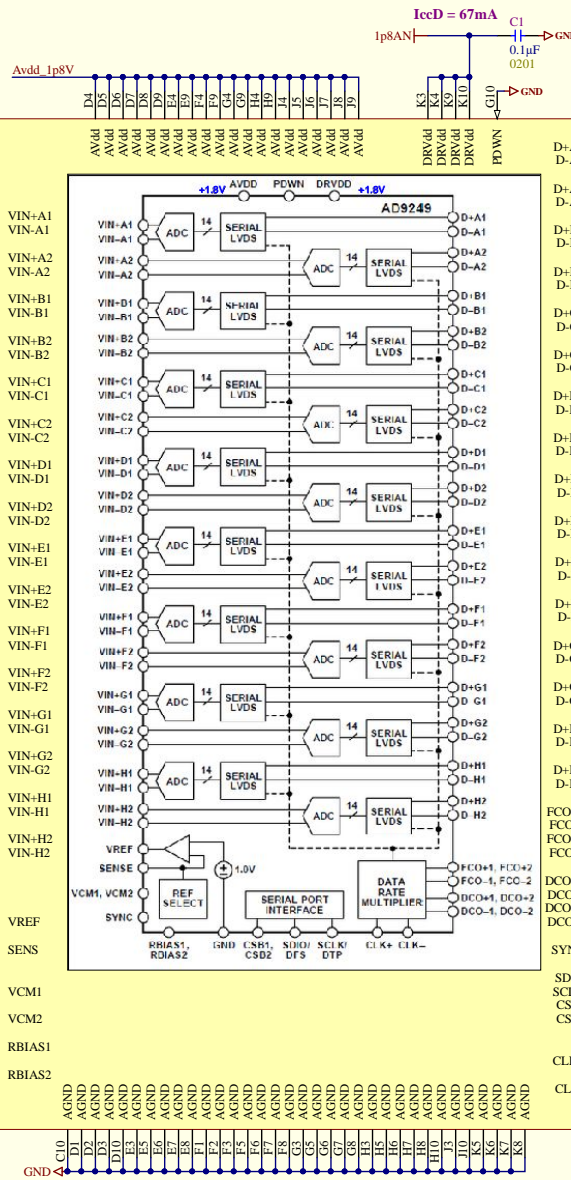
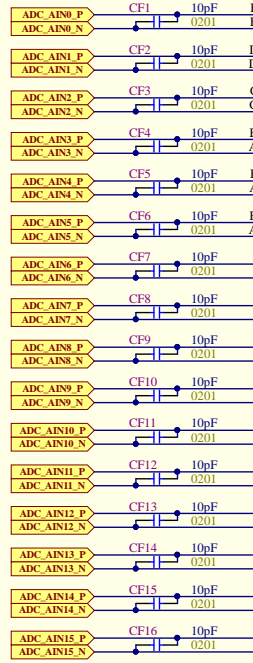




FMC ADC32 - Dual Amp - ADA4950-2YCPZ			
Revision	Drawing #: 7		<b>TRIUMF</b> 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3
<b>1</b>	Sheet #: 7 of 8	Size: A	
	Drawn by: D.Bishop	Date: 3/10/2018	
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**ADC**  
Analog Devices  
AD9249BBCZ-65

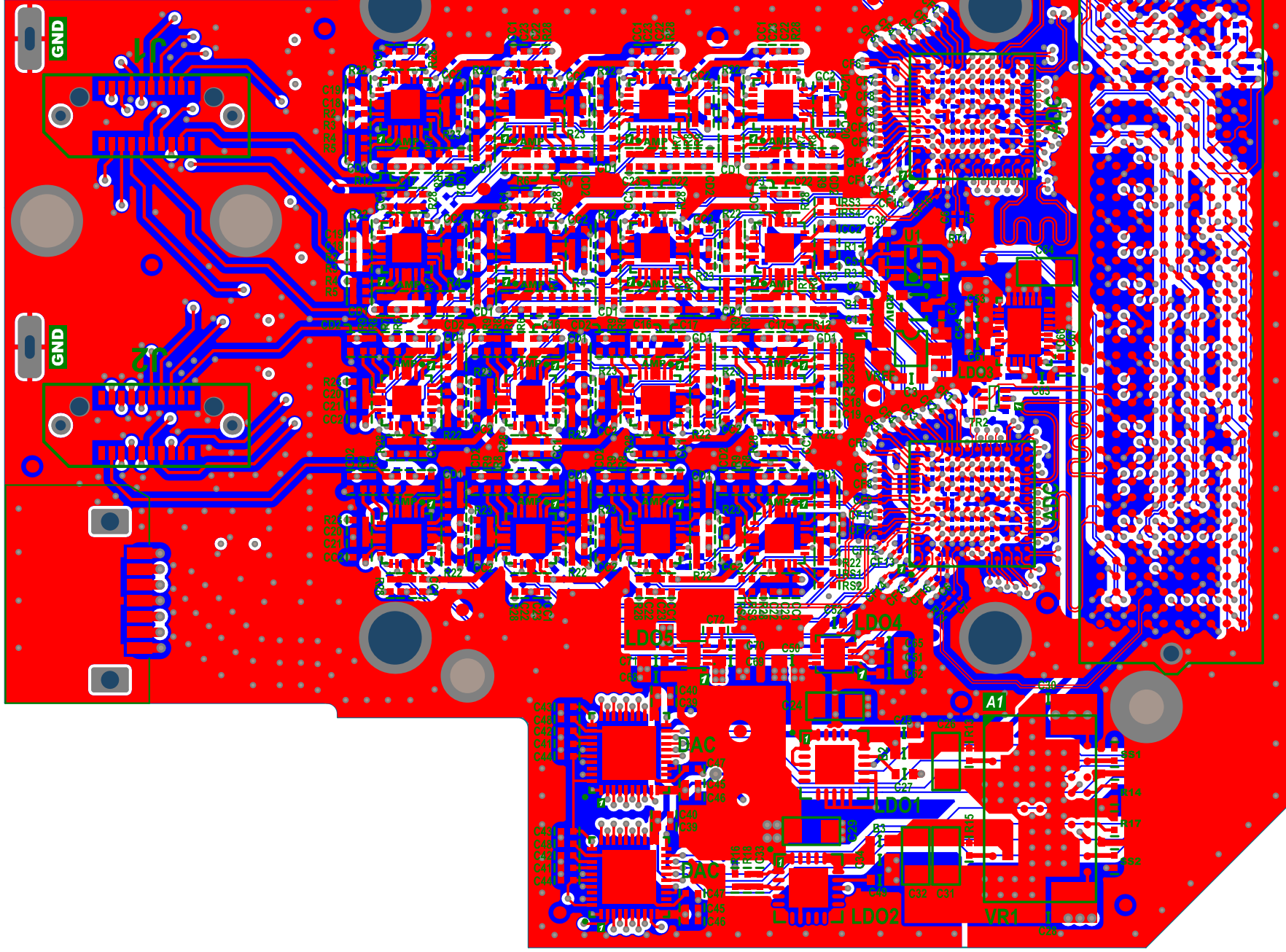


**FMC ADC32 - AD9249 65MSPS - 16 Channel ADC**

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	Drawn by: D.Bishop	Canada
	Date: 3/10/2018	LVT 2A3
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Top Layer (Lyr1)

Top Overlay

Bottom Layer (Lyr10)

