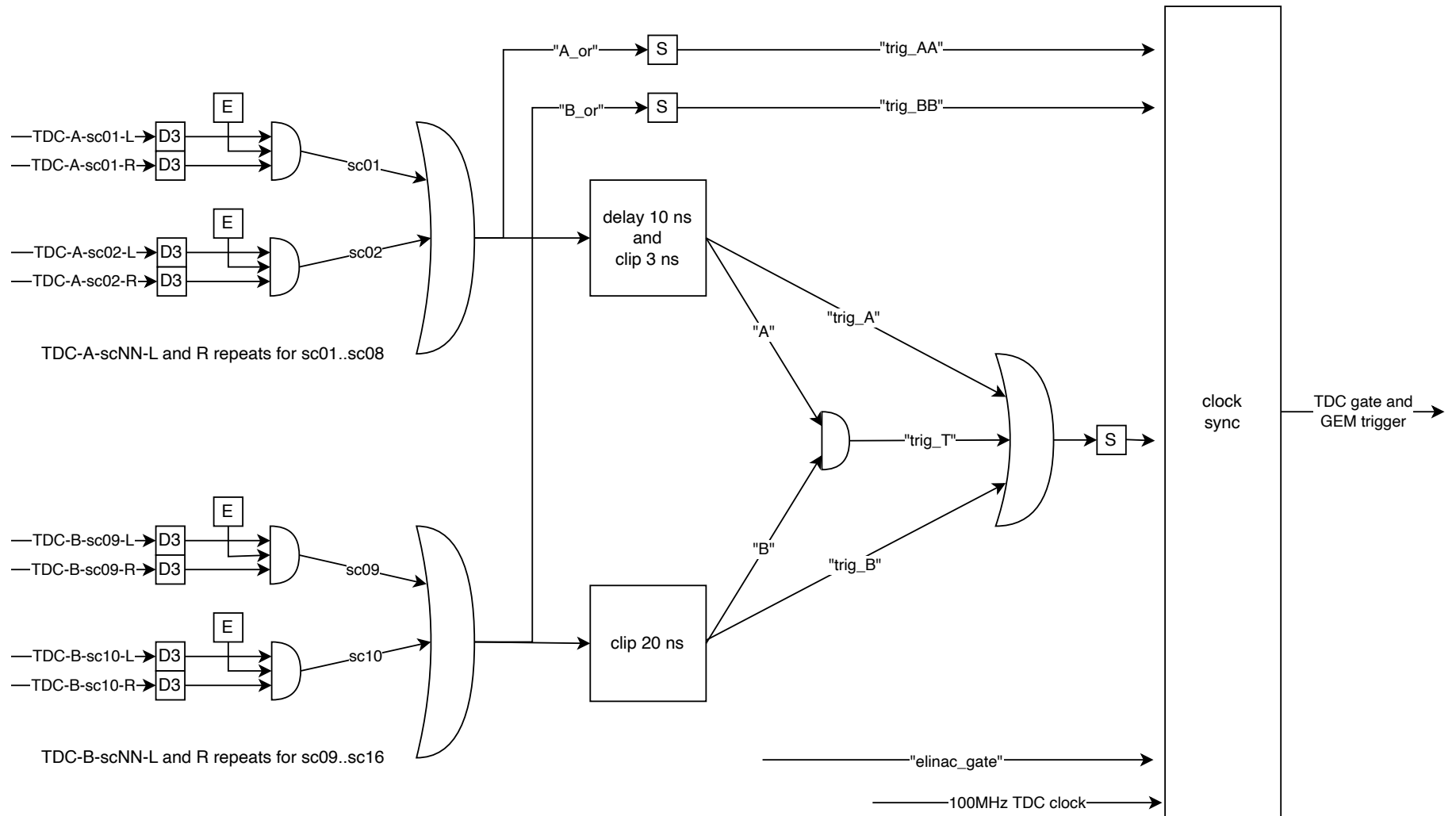


DarkLight FPGA trigger logic, 20-Jan-2026, K.O.



Notes:

- "D3" is the FPGA input pin delay, 7 steps of 0.3 ns, set at compile time, some channels have additional wire delays
- "E" is the "trigger enable" bits from ODB dl_trg_mask
- "S" is a scaledown
- "W" is a wire delay
- "delay and clip" will be constructed from discrete logic to time the electron-position coincidence, set at compile time