
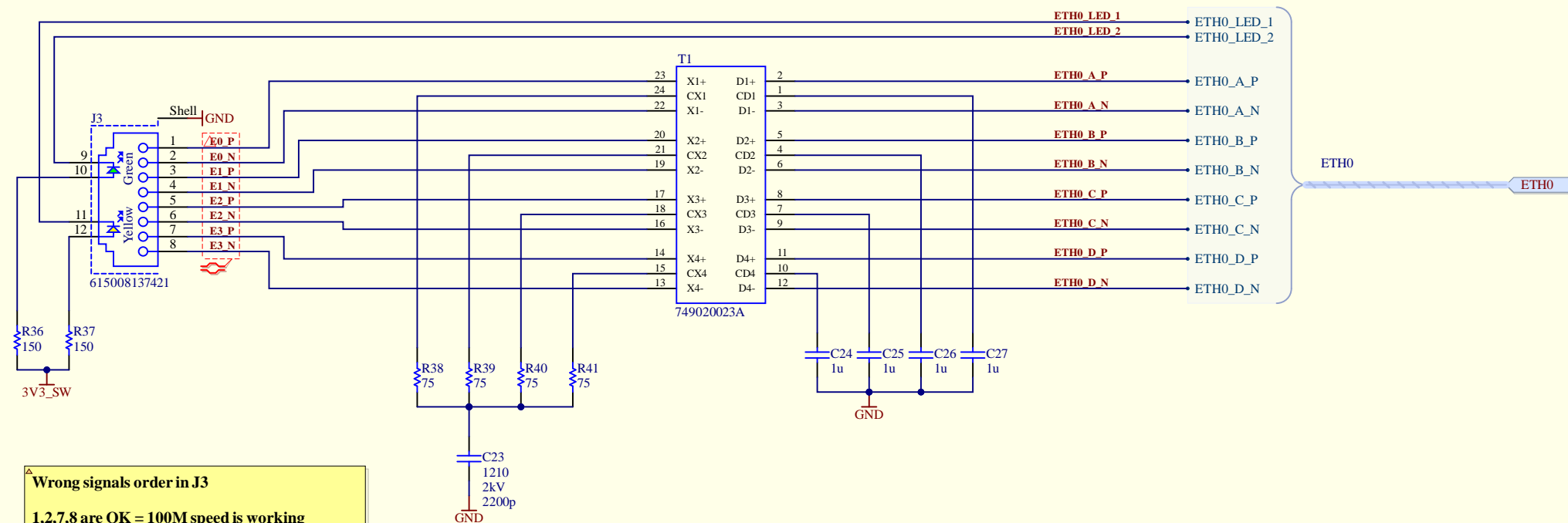
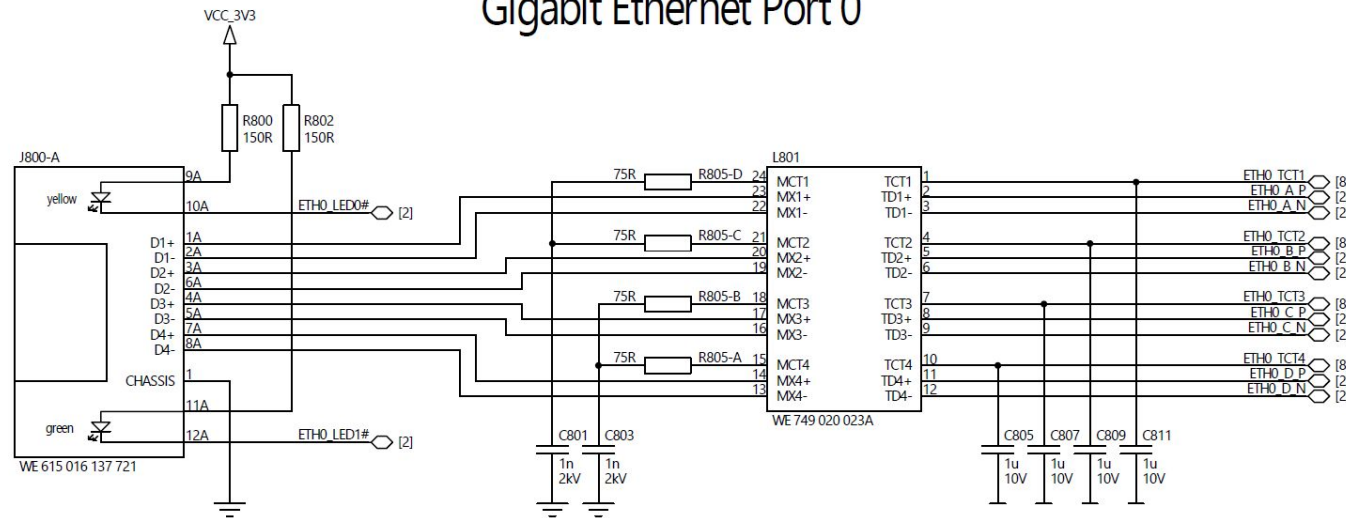


DarkSide - DataManager - SFP

Revision	Drawing #: *		TRIUMF 4004 Wesbrook Mall Vancouver, B.C. Canada V6T 2A3	
0	Sheet #: 3 of 10	Size: A		
Drawn by: *	Date: 2022-10-19			
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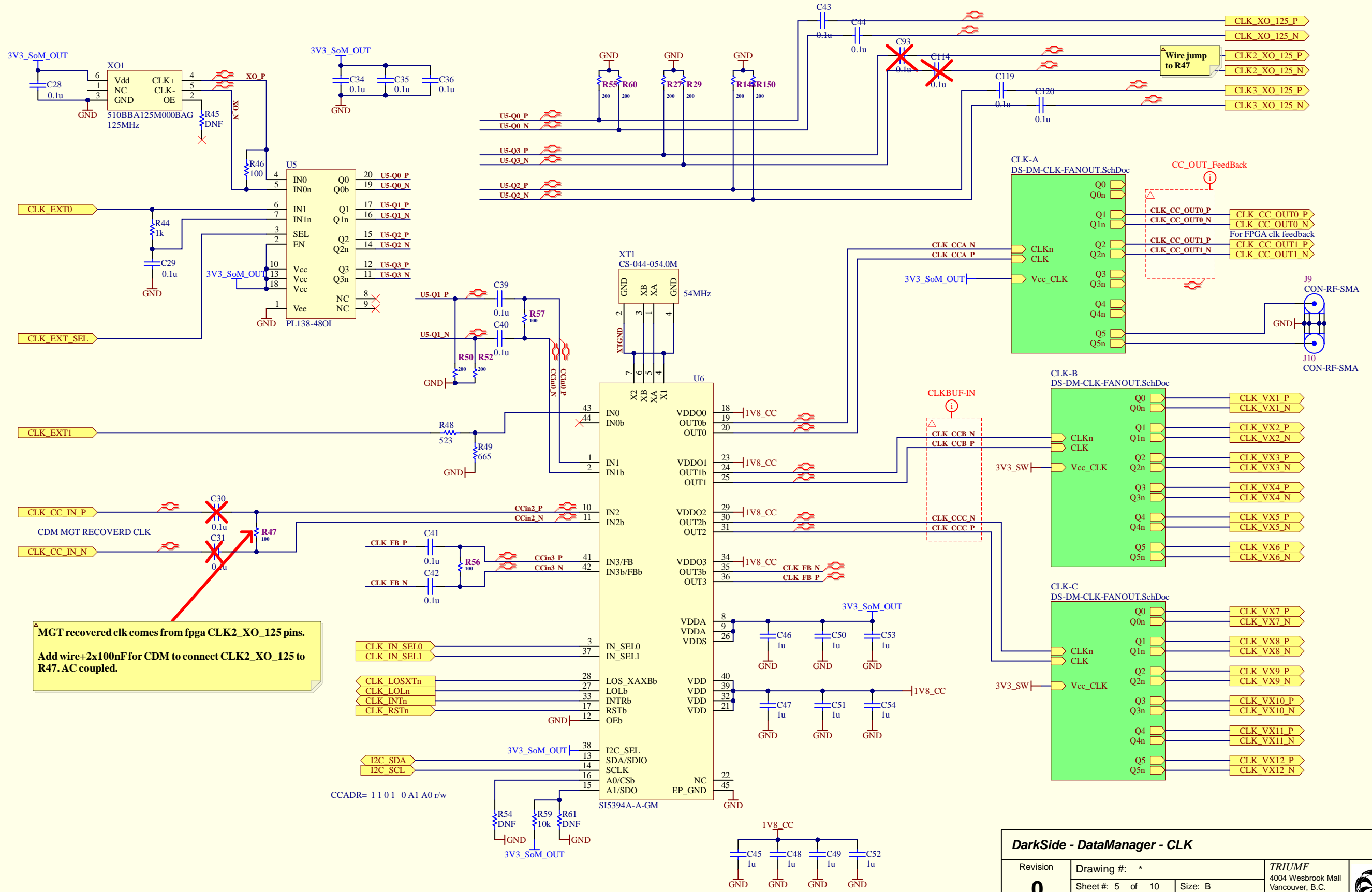
Gigabit Ethernet Port 0



Wrong signals order in J3

1,2,7,8 are OK = 100M speed is working
 3 is OK
 4,5,6 must be reordered - see picture in xls for notes for REV1

HW rework possible - done on SN6
 Other SNx - use special CAT5e cable

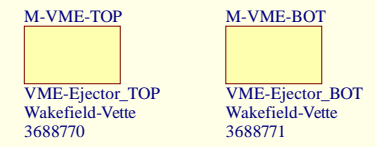
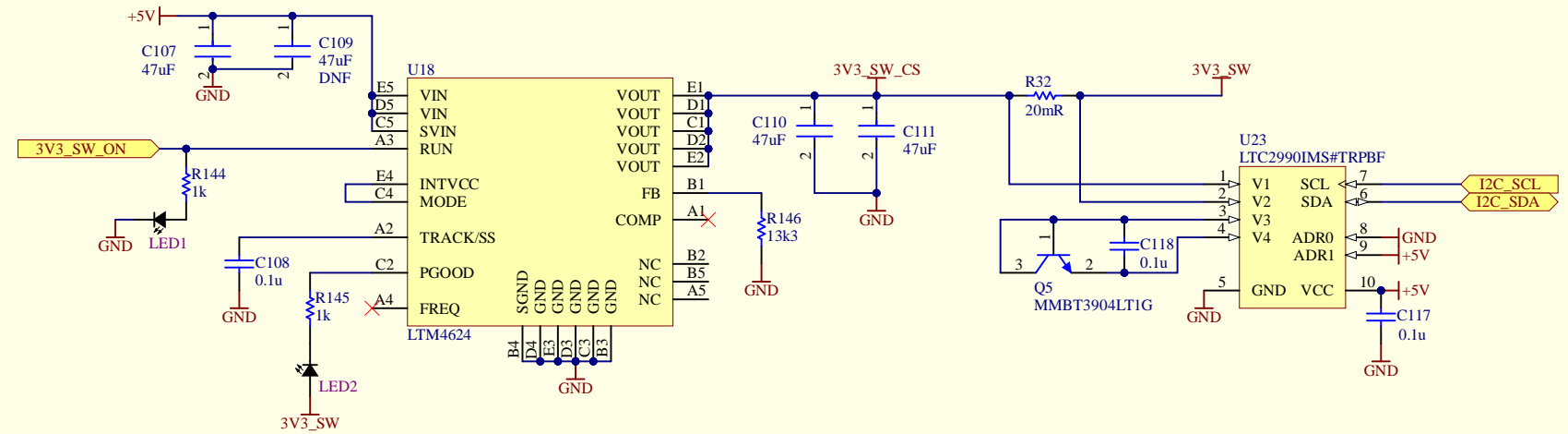
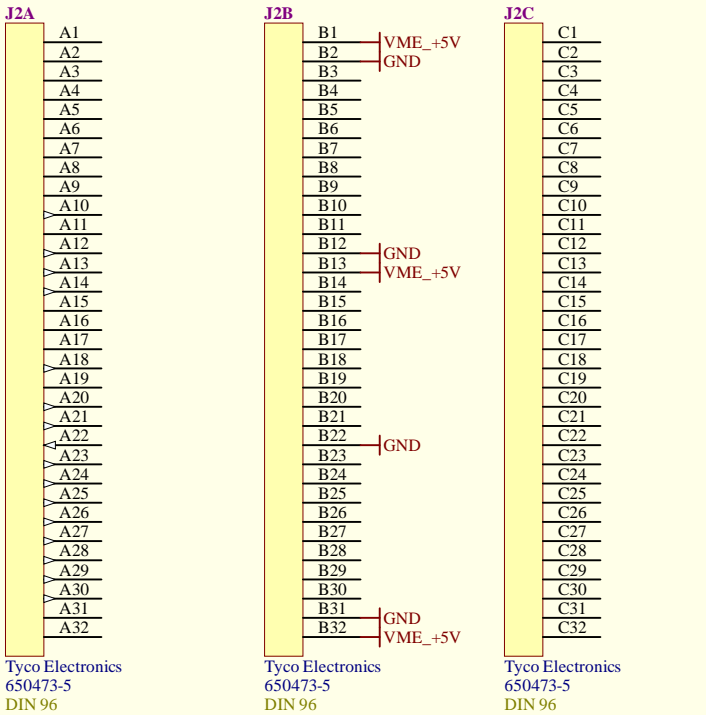
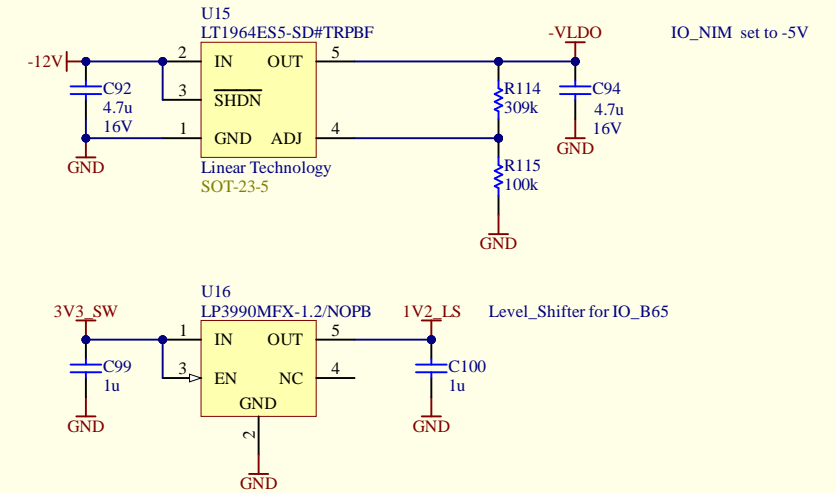
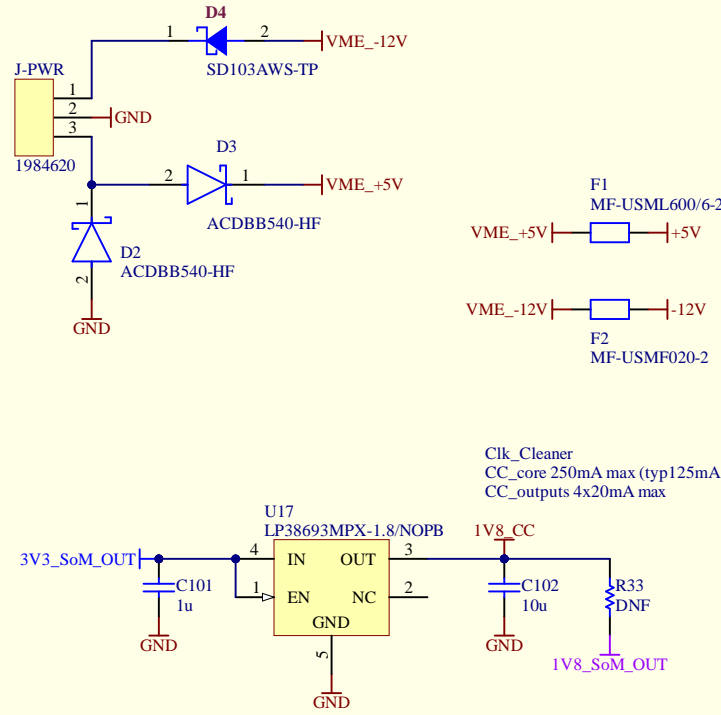
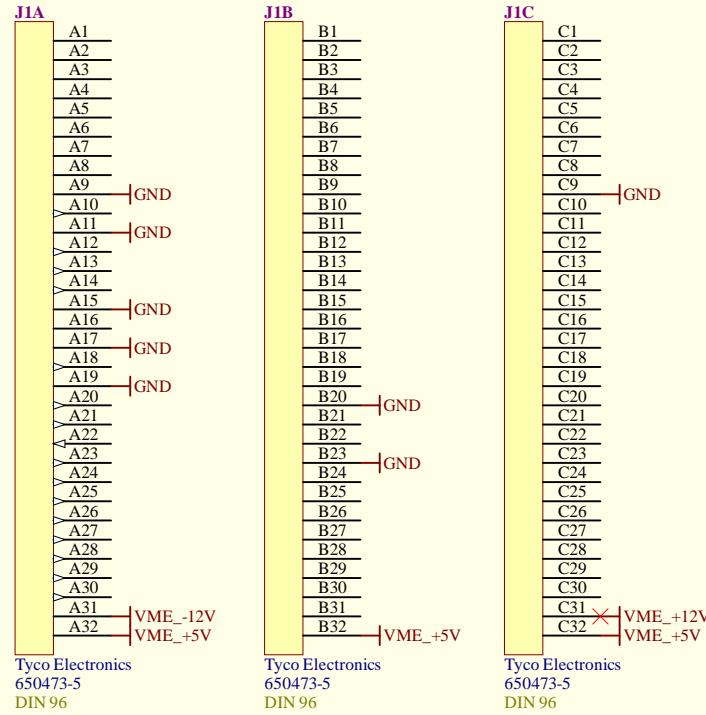


A MGT recovered clk comes from fpga CLK2_XO_125 pins.
 Add wire+2x100nF for CDM to connect CLK2_XO_125 to R47. AC coupled.

File: C:\Work\DarkSide 20k\rev0\Altium\DS-DM-CLK.SchDoc

Current budget 3V3_SW:

Sheet	Current mA	Notes
QSFP/SFP	1800	4x Qsfp each 1.5W (or 1xSFP)
CLK	480	clkcleaner 330mA, XO 100mA, clkbuf 50mA
CLK-FANOUT	1100	750mA = 3x clkbuf static; 18x 20mA each channel out
IO	140	20mA/buf
VX	430	RXbuf 6x22mA + TXbuf 6x50mA

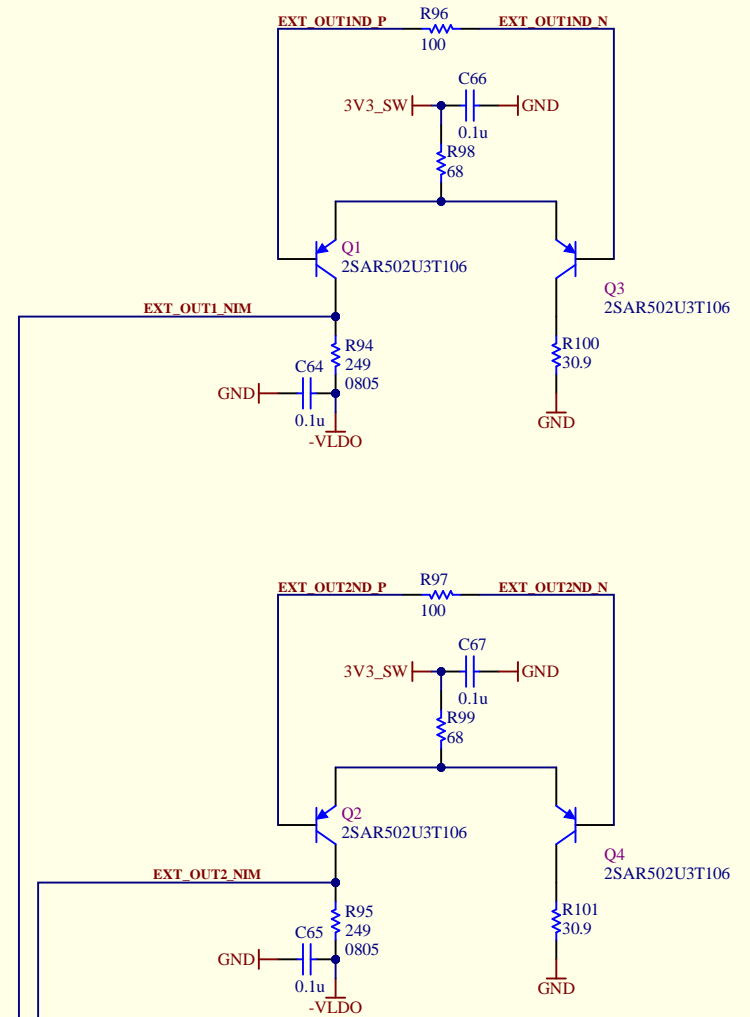
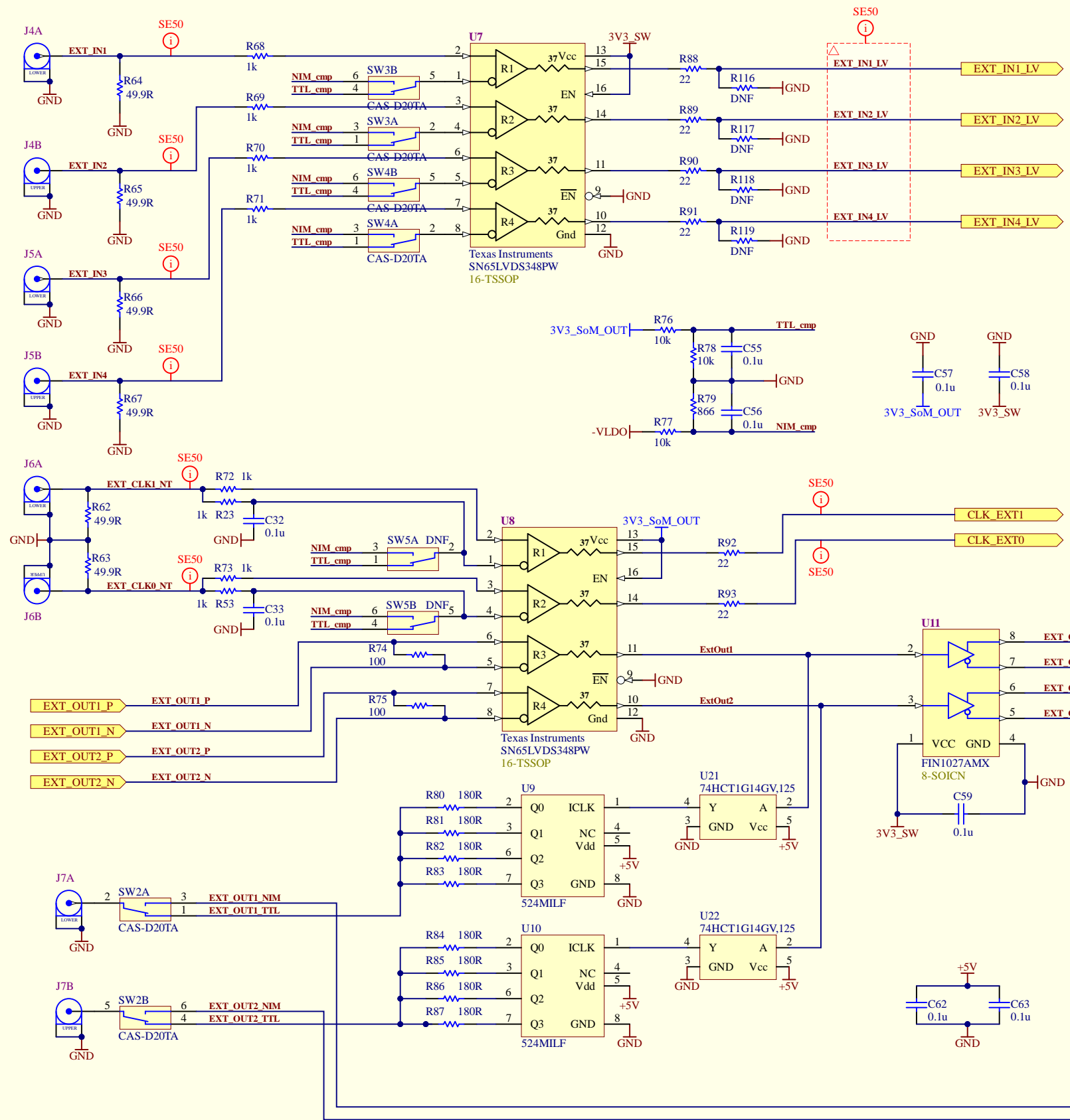


DarkSide - DataManager - Power


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Drawn by: *	Date: 2022-10-19	

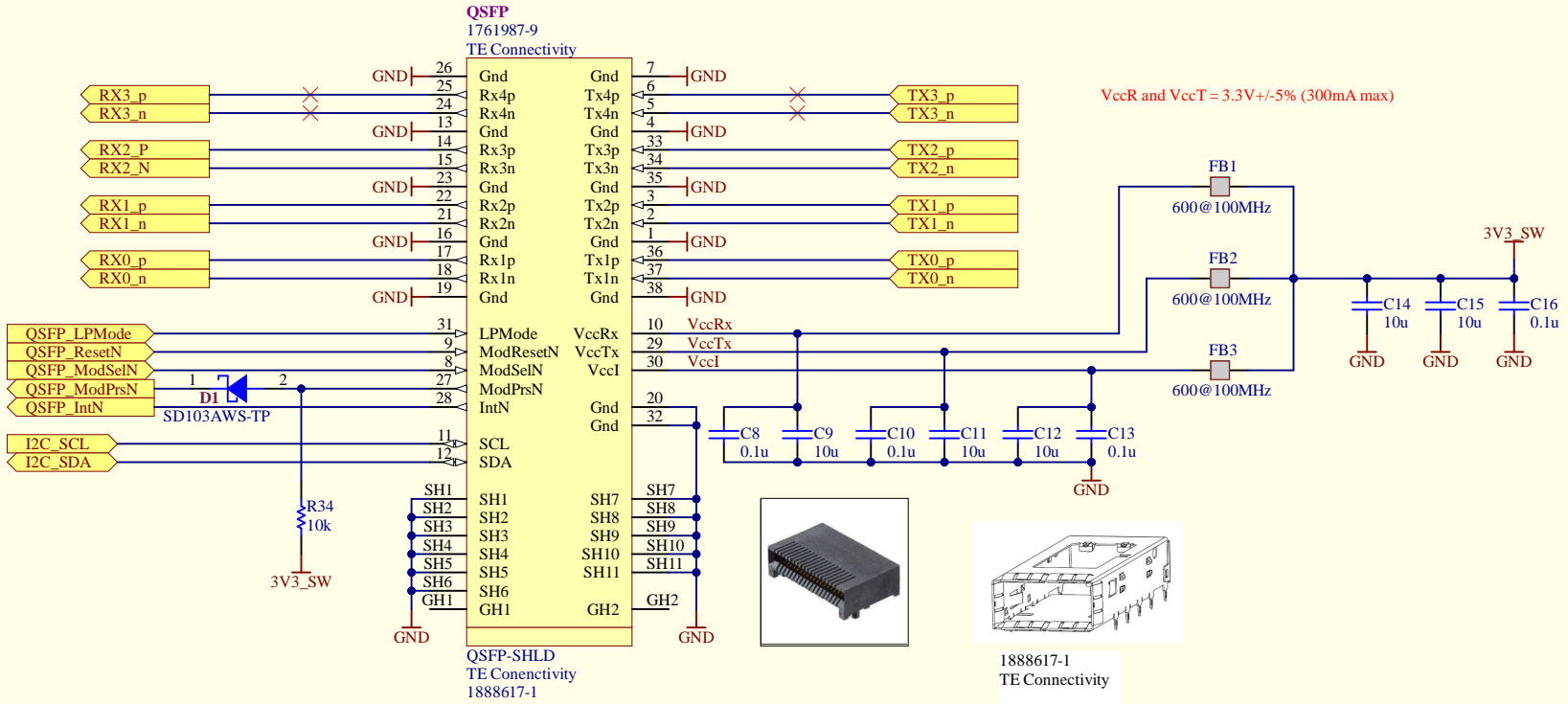
4004 Wesbrook Mall
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Canada
V6T 2A3

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DarkSide - DataManager - CLK

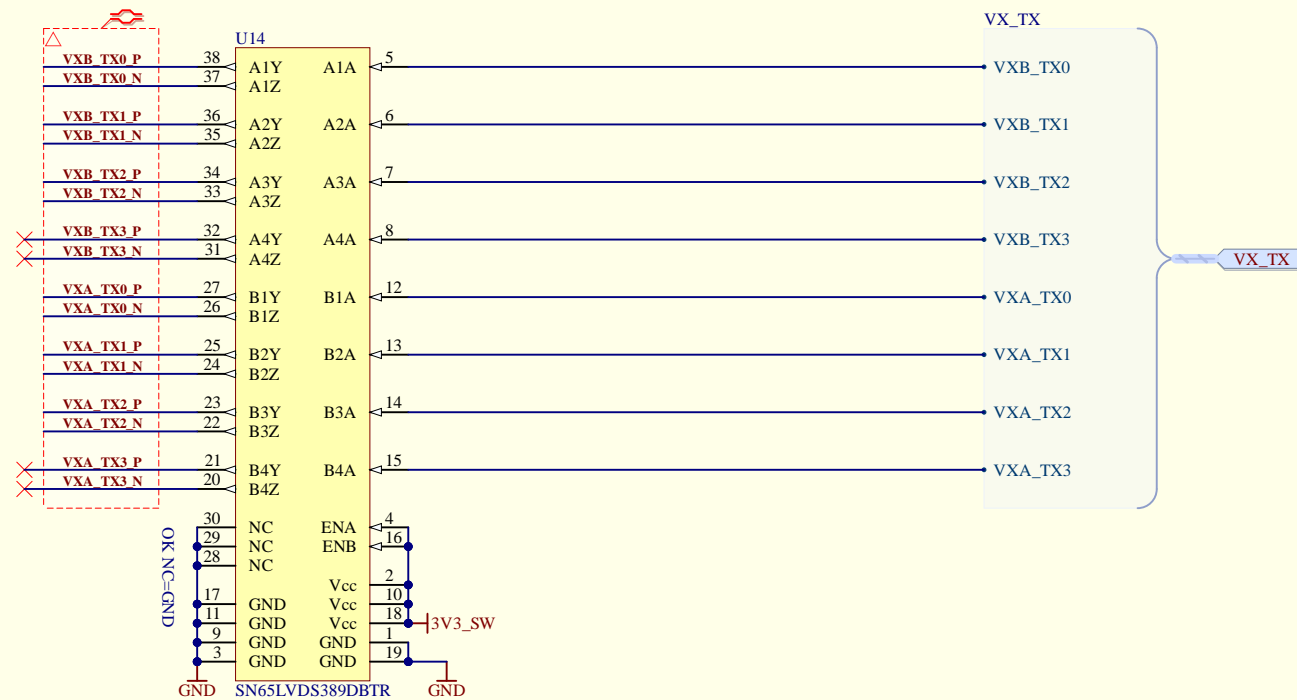
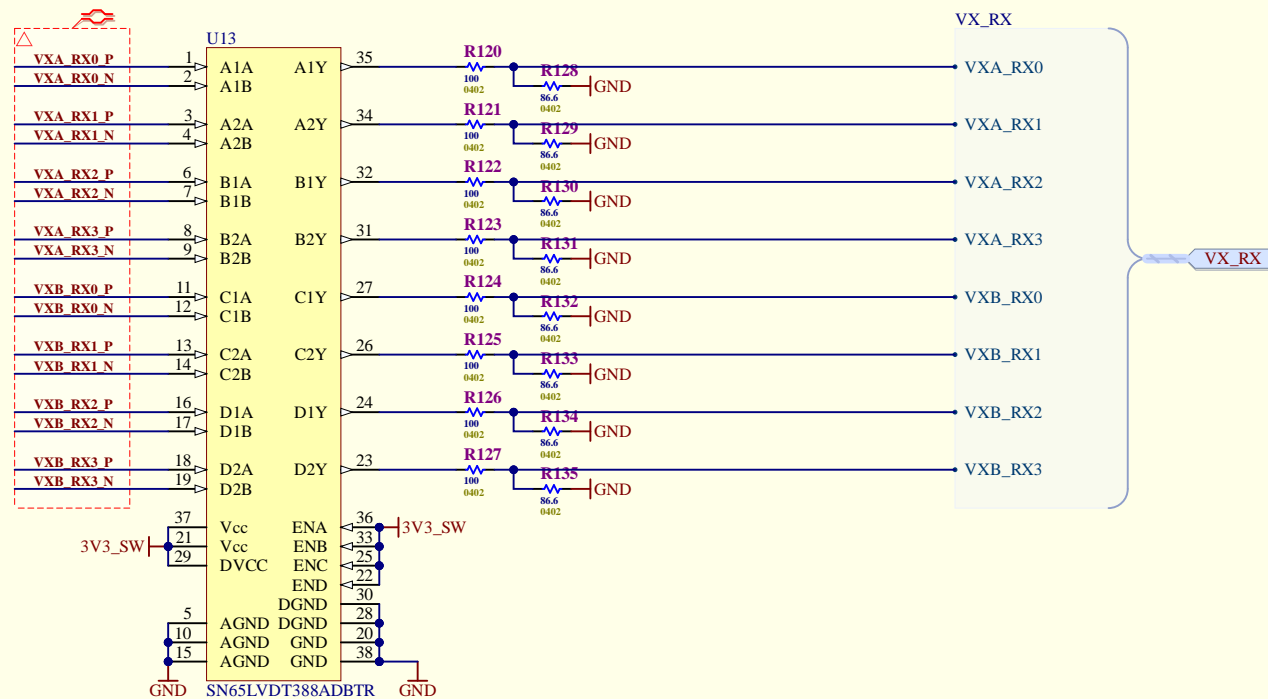
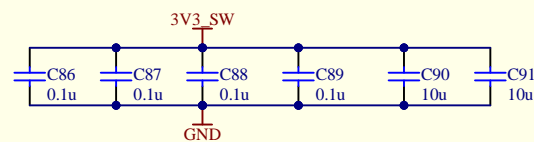
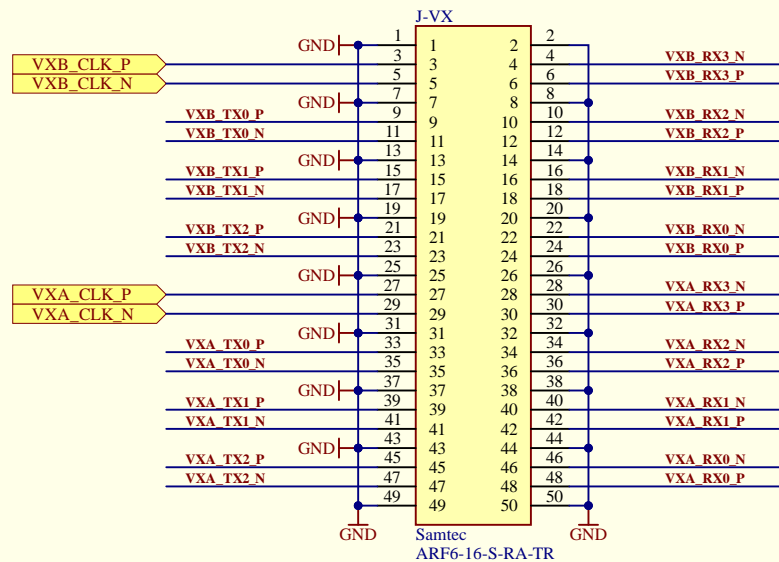
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DarkSide - DataManager - QSFP

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DarkSide - DataManager - VX

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	Drawn by: *	Date: 2022-10-19	