

# TLV5625

## 2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

SLAS233D – JULY 1999 – REVISED JULY 2002

### features

- Dual 8-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time
  - 3  $\mu$ s in Fast Mode
  - 10  $\mu$ s in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity <0.2 LSB Max
- Monotonic Over Temperature

### applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

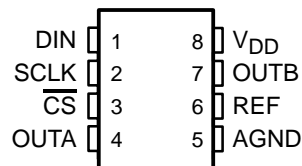
### description

The TLV5625 is a dual 8-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface is compatible with TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 8 data bits.

The resistor string output voltage is buffered by an x2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation.

Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package in standard commercial and industrial temperature ranges.

D PACKAGE  
(TOP VIEW)



AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE
	SOIC (D)
0°C to 70°C	TLV5625CD
–40°C to 85°C	TLV5625ID



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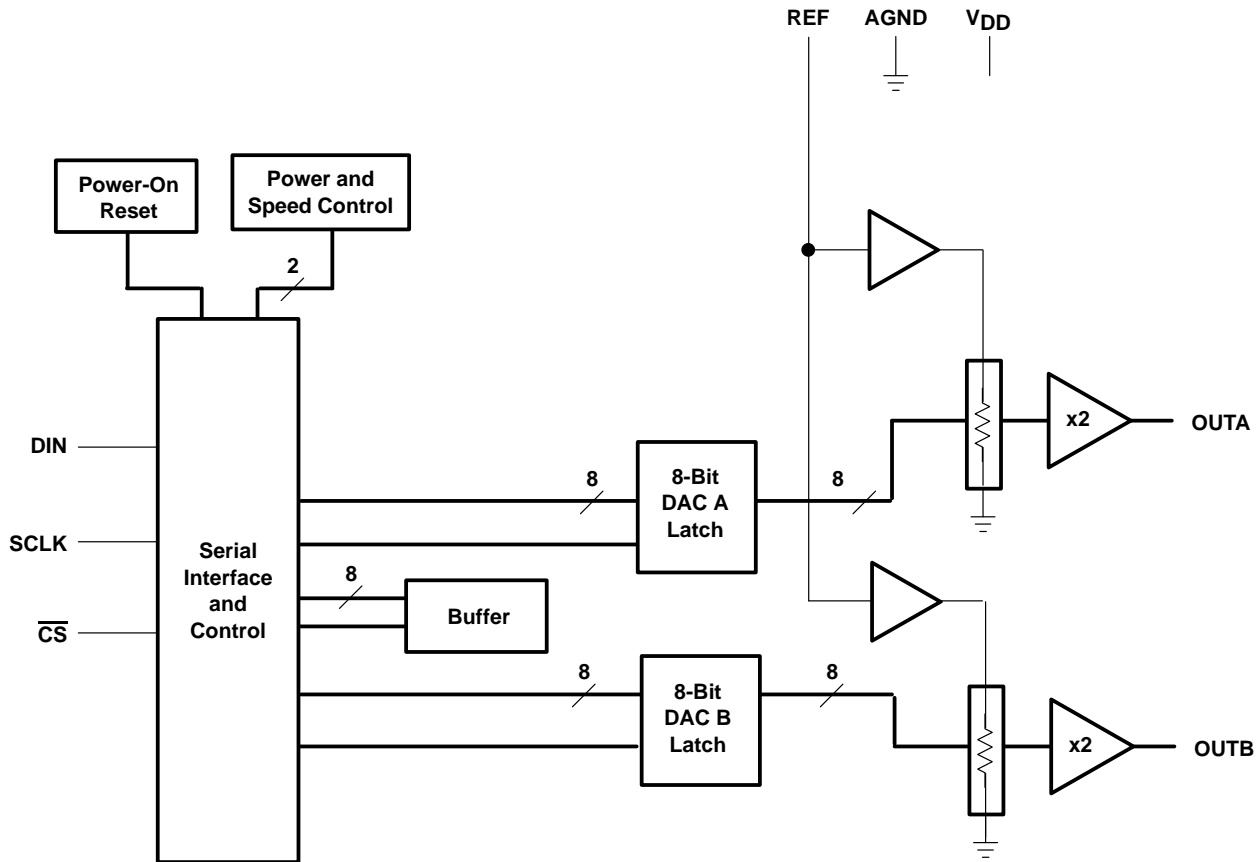
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**functional block diagram**



**Terminal Functions**

TERMINAL NAME	NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{\text{CS}}$	3	I	Chip select. Digital input active low, used to enable/disable inputs.
DIN	1	I	Digital serial data input
OUTA	4	O	DAC A analog voltage output
OUTB	7	O	DAC B analog voltage output
REF	6	I	Analog reference voltage input
SCLK	2	I	Digital serial clock input
VDD	8	P	Positive power supply



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ( $V_{DD}$ to AGND)	7 V
Reference input voltage range	– 0.3 V to $V_{DD} + 0.3$ V
Digital input voltage range	– 0.3 V to $V_{DD} + 0.3$ V
Operating free-air temperature range, $T_A$ : TLV5625C	0°C to 70°C
TLV5625I	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$	$V_{DD} = 5$ V	4.5	5	5.5	V
	$V_{DD} = 3$ V	2.7	3	3.3	
Power on reset, POR		0.55		2	V
High-level digital input voltage, $V_{IH}$	$V_{DD} = 2.7$ V	2			V
	$V_{DD} = 5.5$ V	2.4			
Low-level digital input voltage, $V_{IL}$	$V_{DD} = 2.7$ V			0.6	V
	$V_{DD} = 5.5$ V			1	
Reference voltage, $V_{ref}$ to REF terminal	$V_{DD} = 5$ V (see Note 1)	AGND	2.048	$V_{DD} - 1.5$	V
	$V_{DD} = 3$ V (see Note 1)	AGND	1.024	$V_{DD} - 1.5$	V
Load resistance, $R_L$		2			k $\Omega$
Load capacitance, $C_L$				100	pF
Clock frequency, $f_{CLK}$				20	MHz
Operating free-air temperature, $T_A$	TLV5625C	0		70	°C
	TLV5625I	–40		85	

NOTE 1: Due to the x2 output buffer, a reference input voltage  $\geq (V_{DD} - 0.4$  V)/2 causes clipping of the transfer function.

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### electrical characteristics over recommended operating conditions (unless otherwise noted)

#### power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD</sub>	Power supply current	No load, All inputs = AGND or V <sub>DD</sub> , DAC latch = 0x800	Fast	1.8	2.3	mA
			Slow	0.8	1	
	Power-down supply current			1	3	μA
PSRR	Power supply rejection ratio	Zero scale, See Note 2		-65		dB
		Full scale, See Note 3		-65		

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V<sub>DD</sub> and is given by:

$$PSRR = 20 \log [(E_{ZS}(V_{DDmax}) - E_{ZS}(V_{DDmin})/V_{DDmax}]$$

3. Power supply rejection ratio at full scale is measured by varying V<sub>DD</sub> and is given by:

$$PSRR = 20 \log [(E_G(V_{DDmax}) - E_G(V_{DDmin})/V_{DDmax}]$$

#### static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8			bits
INL	Integral nonlinearity	See Note 4		±0.3	±0.5	LSB
DNL	Differential nonlinearity	See Note 5		±0.07	±0.2	LSB
E <sub>ZS</sub>	Zero-scale error (offset error at zero scale)	See Note 6			±12	mV
E <sub>ZS TC</sub>	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
E <sub>G</sub>	Gain error	See Note 8			±0.5	% full scale V
E <sub>G TC</sub>	Gain-error temperature coefficient	See Note 9		10		ppm/°C

NOTES: 4. The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero-code and full-scale errors.

5. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes.

6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.

7. Zero-scale error temperature coefficient is given by:  $E_{ZS TC} = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/2V_{ref} \times 10^6/(T_{max} - T_{min})$ .

8. Gain error is the deviation from the ideal output (2V<sub>ref</sub> - 1 LSB) with an output load of 10 kΩ.

9. Gain temperature coefficient is given by:  $E_{G TC} = [E_G(T_{max}) - E_G(T_{min})]/2V_{ref} \times 10^6/(T_{max} - T_{min})$ .

#### output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>O</sub>	Output voltage range	R <sub>L</sub> = 10 kΩ	0	V <sub>DD</sub> -0.4		V
	Output load regulation accuracy	V <sub>O</sub> = 4.096 V, 2.048 V R <sub>L</sub> = 2 kΩ			±0.29	% FS

#### reference input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>I</sub>	Input voltage range		0	V <sub>DD</sub> -1.5		V
R <sub>I</sub>	Input resistance			10		MΩ
C <sub>I</sub>	Input capacitance			5		pF
Reference input bandwidth	REF = 0.2 V <sub>pp</sub> + 1.024 V dc	Fast		1.3		MHz
		Slow		525		kHz
Reference feedthrough	REF = 1 V <sub>pp</sub> at 1 kHz + 1.024 V dc (see Note 10)			-80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.



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**electrical characteristics over recommended operating conditions (unless otherwise noted)**  
**(Continued)**

**digital inputs**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH}$	High-level digital input current	$V_I = V_{DD}$			1	$\mu A$
$I_{IL}$	Low-level digital input current	$V_I = 0 V$	-1			$\mu A$
$C_i$	Input capacitance			8		pF

**analog output dynamic performance**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_s(FS)$	Output settling time, full scale	$R_L = 10 k\Omega$ , See Note 11	$C_L = 100 pF$ ,	Fast	1	3	$\mu s$
				Slow	3	10	
$t_s(CC)$	Output settling time, code to code	$R_L = 10 k\Omega$ , See Note 12	$C_L = 100 pF$ ,	Fast	1		$\mu s$
				Slow	2		
SR	Slew rate	$R_L = 10 k\Omega$ , See Note 13	$C_L = 100 pF$ ,	Fast	3		V/ $\mu s$
				Slow	0.5		
Glitch energy		$\overline{DIN} = 0$ to 1, $\overline{CS} = V_{DD}$	FCLK = 100 kHz,		5		nV-s
SNR	Signal-to-noise ratio	$f_s = 102 kSPS$ , $R_L = 10 k\Omega$ ,	$f_{out} = 1 kHz$ , $C_L = 100 pF$		52	54	dB
SINAD	Signal-to-noise + distortion				48	49	
THD	Total harmonic distortion				-50	-48	
SFDR	Spurious free dynamic range				48	50	

- NOTES: 11. Settling time is the time for the output signal to remain within  $\pm 0.5$  LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.  
12. Settling time is the time for the output signal to remain within  $\pm 0.5$  LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.  
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full-scale voltage.



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**digital input timing requirements**

	MIN	NOM	MAX	UNIT
$t_{su}(CS-CK)$ Setup time, $\overline{CS}$ low before first negative SCLK edge	10			ns
$t_{su}(C16-CS)$ Setup time, 16 <sup>th</sup> negative SCLK edge before $\overline{CS}$ rising edge	10			ns
$t_{wH}$ SCLK pulse width high	25			ns
$t_{wL}$ SCLK pulse width low	25			ns
$t_{su}(D)$ Setup time, data ready before SCLK falling edge	10			ns
$t_h(D)$ Hold time, data held valid after SCLK falling edge	10			ns

**timing requirements**

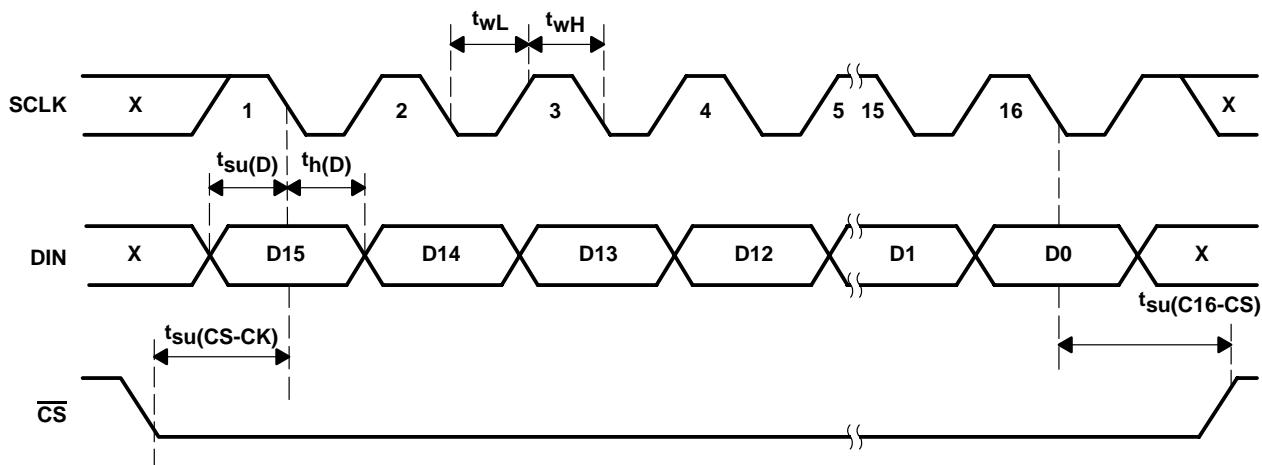


Figure 1. Timing Diagram

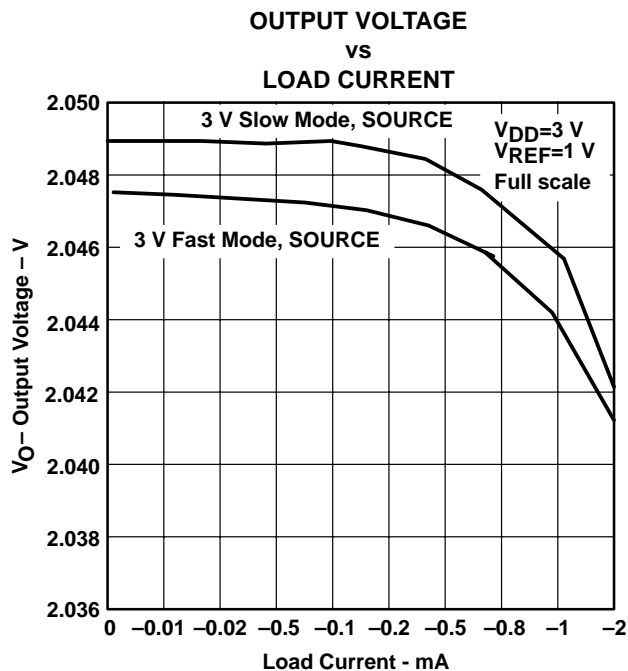


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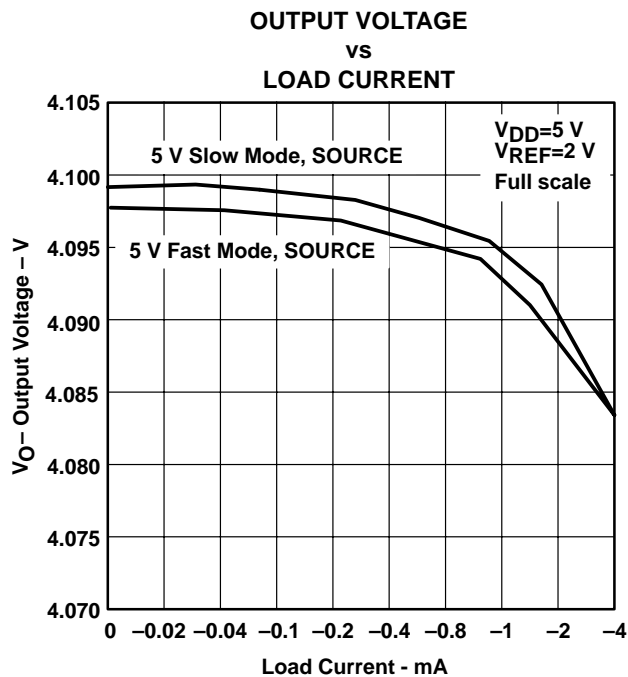
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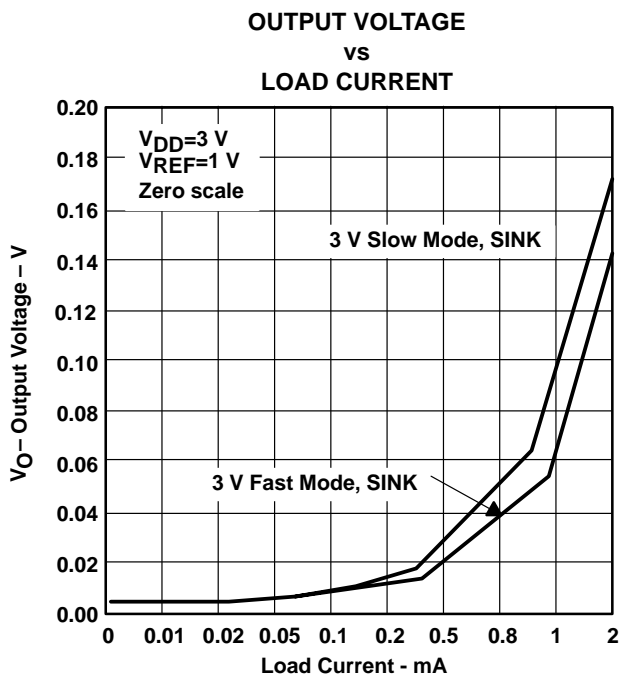
### TYPICAL CHARACTERISTICS



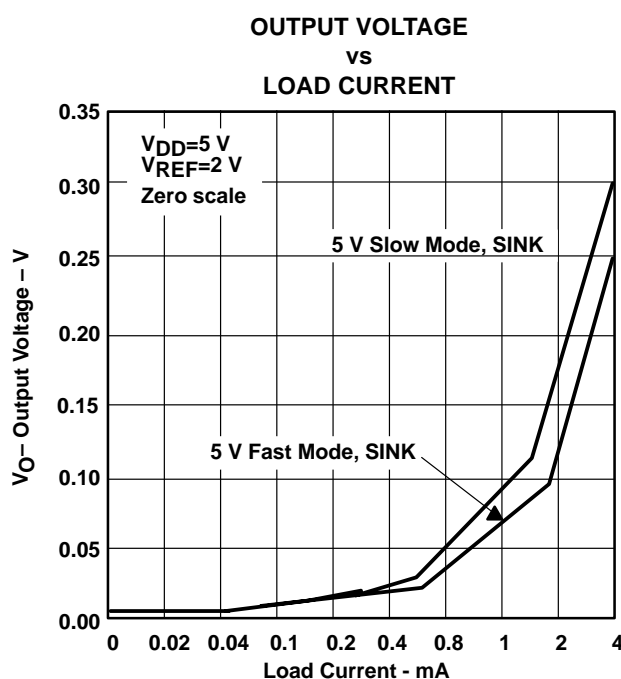
**Figure 2**



**Figure 3**



**Figure 4**



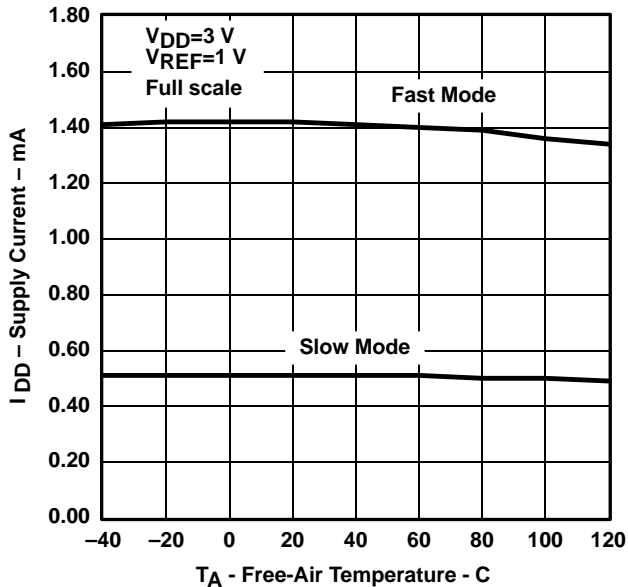
**Figure 5**

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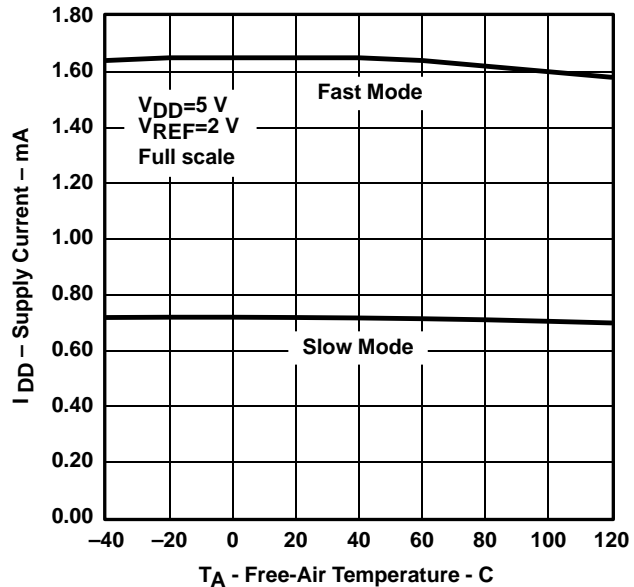
**TYPICAL CHARACTERISTICS**

**SUPPLY CURRENT**  
**vs**  
**FREE-AIR TEMPERATURE**



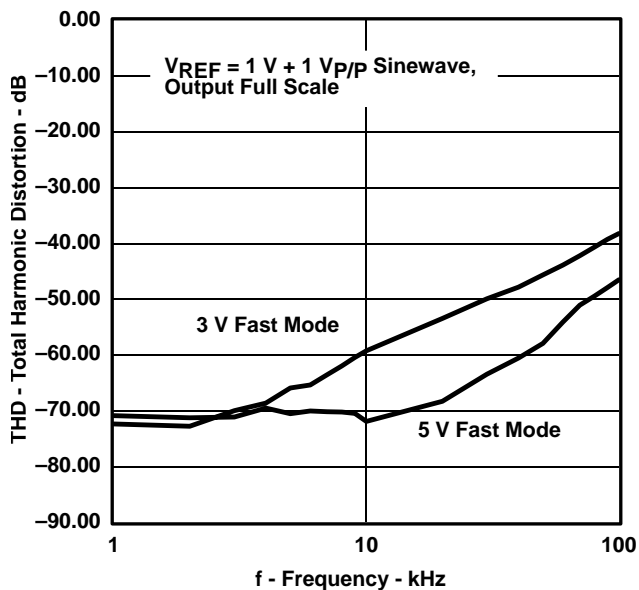
**Figure 6**

**SUPPLY CURRENT**  
**vs**  
**FREE-AIR TEMPERATURE**



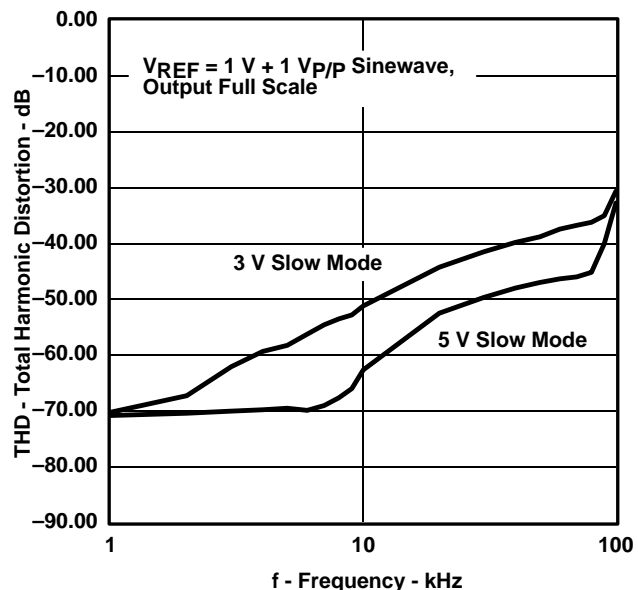
**Figure 7**

**TOTAL HARMONIC DISTORTION**  
**vs**  
**FREQUENCY**



**Figure 8**

**TOTAL HARMONIC DISTORTION**  
**vs**  
**FREQUENCY**



**Figure 9**





TYPICAL CHARACTERISTICS

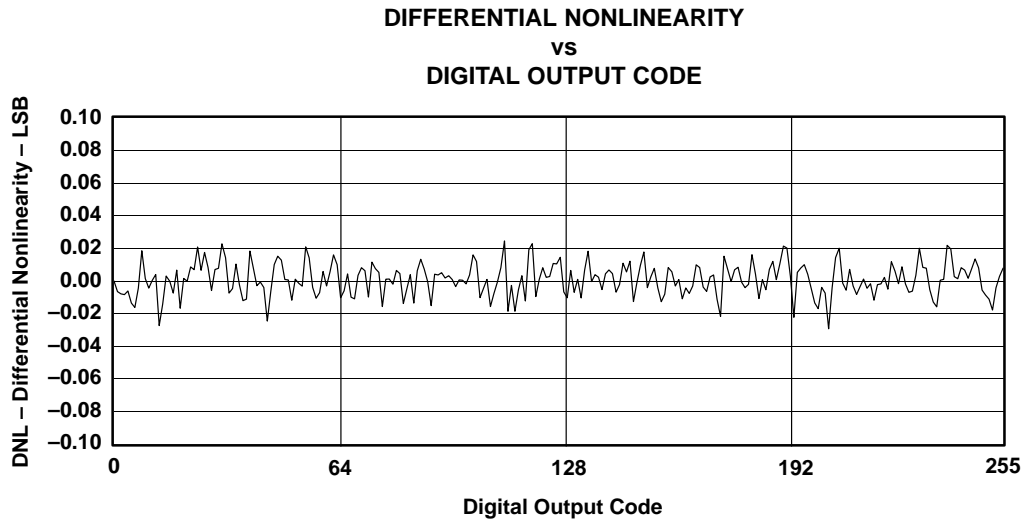


Figure 10

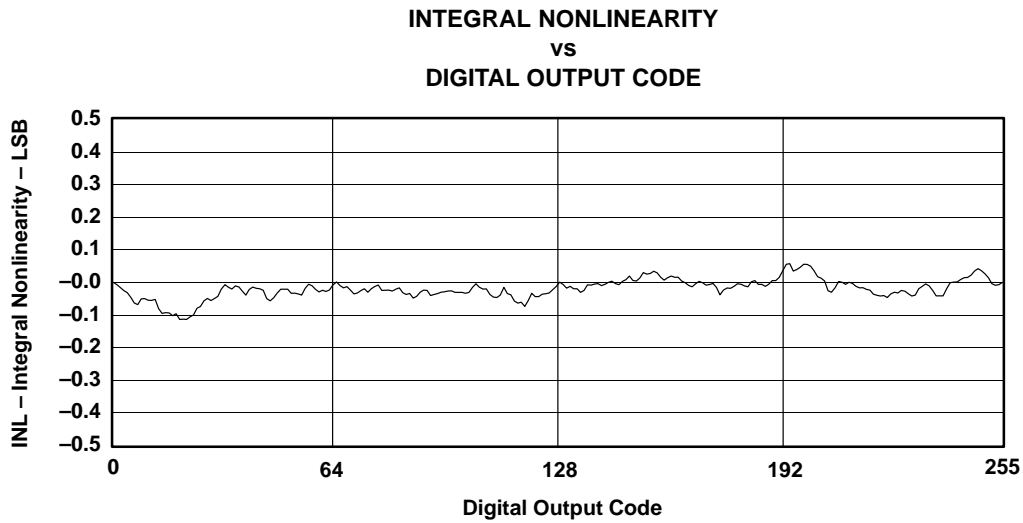


Figure 11

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### APPLICATION INFORMATION

#### general function

The TLV5625 is a dual 8-bit, single-supply DAC, based on a resistor-string architecture. It consists of a serial interface, a speed and power-down control logic, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by the reference) is given by:

$$2 \text{ REF} \frac{\text{CODE}}{2^n} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value within the range of  $0_{10}$  to  $2^n-1$ , where  $n=8$  (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

#### serial interface

A falling edge of  $\overline{\text{CS}}$  starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or  $\overline{\text{CS}}$  rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 2 shows examples of how to connect the TLV5625 to TMS320, SPI™, and Microwire™.

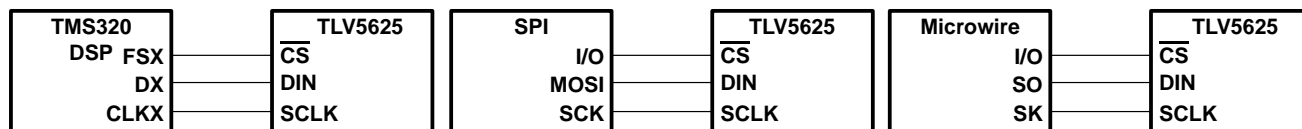


Figure 12. Three-Wire Interface

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to  $\overline{\text{CS}}$ . If the word width is 8 bits (SPI™ and Microwire™) two write operations must be performed to program the TLV5625. After the write operation(s), the holding registers or the control register are updated automatically on the 16<sup>th</sup> positive clock edge.

#### serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{\text{sclkmax}} = \frac{1}{t_{\text{whmin}} + t_{\text{wlmin}}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{\text{updatemax}} = \frac{1}{16 (t_{\text{whmin}} + t_{\text{wlmin}})} = 1.25 \text{ MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5625 should also be considered.

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## APPLICATION INFORMATION

### data format

The 16-bit data word for the TLV5625 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D4)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
R1	SPD	PWR	R0	8 Data bits								LSB	0	0	0	0

SPD: Speed control bit    1 → fast mode                                  0 → slow mode  
PWR: Power control bit    1 → power down    0 → normal operation  
On power up, SPD and PWD are reset to 0 (slow mode and normal operation)

The following table lists all possible combination of register-select bits:

### register-select bits

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Reserved

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

### examples of operation

- Set DAC A output, select fast mode:

Write new DAC A value and update DAC A output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A output value								0	0	0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC B output, select fast mode:

Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New BUFFER content and DAC B output value								0	0	0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC A value, set DAC B value, update both simultaneously, select slow mode:

1. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value								0	0	0	0

2. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value								0	0	0	0



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**APPLICATION INFORMATION**

**examples of operation (continued)**

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

- Set power-down mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X

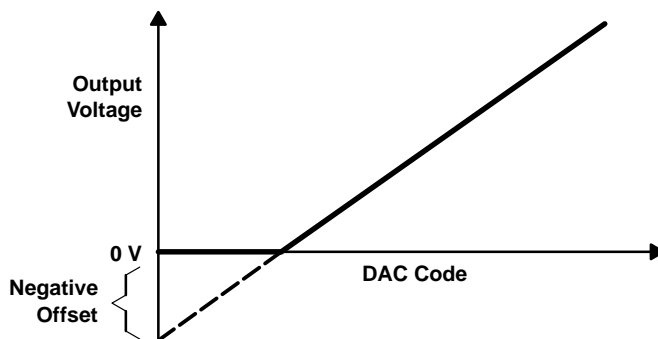
X = Don't care

**linearity, offset, and gain error using single ended supplies**

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 13.



**Figure 13. Effect of Negative Offset (Single Supply)**

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

**power-supply bypassing and ground management**

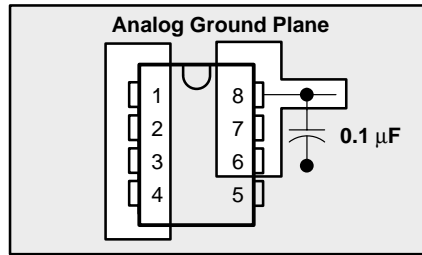
Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- $\mu$ F ceramic-capacitor bypass should be connected between  $V_{DD}$  and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 14 shows the ground plane layout and bypassing technique.



## APPLICATION INFORMATION



**Figure 14. Power-Supply Bypassing**

### definitions of specifications and terminology

#### integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

#### differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

#### zero-scale error ( $E_{ZS}$ )

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

#### gain error ( $E_G$ )

Gain error is the error in slope of the DAC transfer function.

#### signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

#### spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

#### total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

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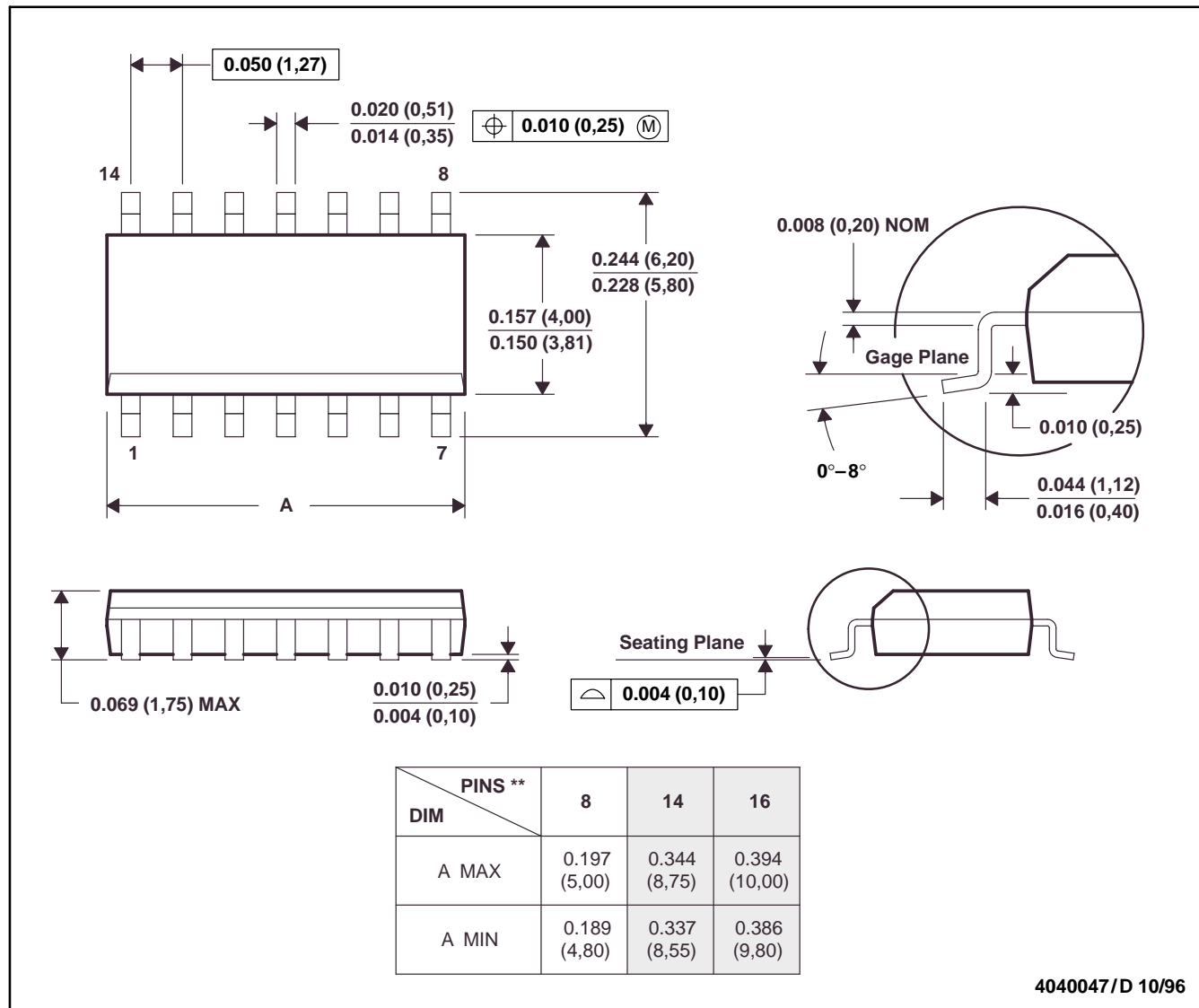
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**MECHANICAL DATA**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

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