W-IE-NE-R CC_USB
CPLD Upgrade

The CC_USB has several CPLDs that can be upgraded by the user. In order to program the CPLD you must first download Xilinx Webpack from their website and have a JTAG adapter. For help with either of these you can contact support@wiener-us.com.

To update the CPLD follow the following steps:

1) Connect the JTAG adapter to the appropriate port on the CC_USB using the pin layout in Appendix A and drawings shown on the following pages.
2) Power up the CC_USB
3) Open Impact.exe directly (click Cancel to get rid of dialog box)
4) Right-click and choose “Initialize Chain” (If you get an error make you have good contact at the JTAG port)
5) You will be asked to choose a file for that device, Choose the file which you want to load onto that CPLD
6) Right-click on the device icon and choose program
7) Select “Verify” before hitting OK
8) After programming is completed close the program and turn off the power to the CC_USB before removing the JTAG connector.

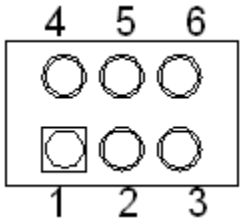
At the time of there are 2 CPLD upgrades possible and recommended:

B1) CPLD files for CC-USB upgrade Broadcast (04/19/2006): for SN<46

B2) Hardware Release 1.0.b delayed FPGA Booting (10/14/2006): for SN<75

Appendix A

JTAG port pin layout



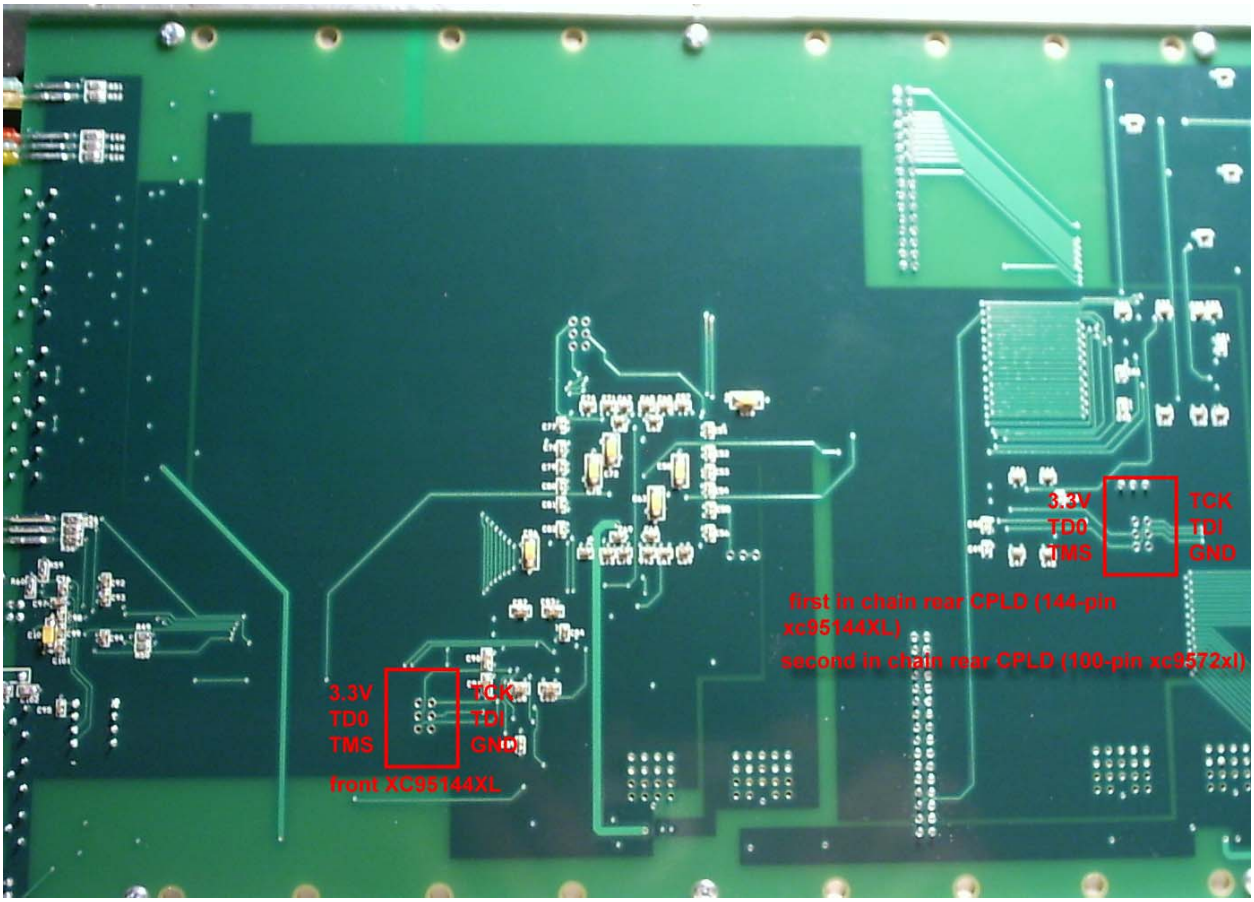
1) **CCLK**
2) **DIN**
3) **GND**
4) **VCC (3.3V)**
5) **D/P**
6) **PROG**

(The JTEC programming adapter has 2 connectors with 3 pins each, which can be plugged on the existing or to the provided header. To match the pins connect the red cable to VCC (pin4) and the black one to GND (pin 3)

Appendix B: CC-USB CPLD Upgrades

B1) CPLD files for CC-USB upgrade Broadcast (04/19/2006):

B1.1) Newer Units: Soldering side of Slot 25 (to be used for upgrade for units without header)

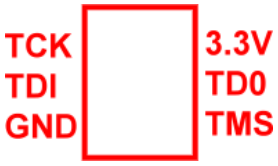


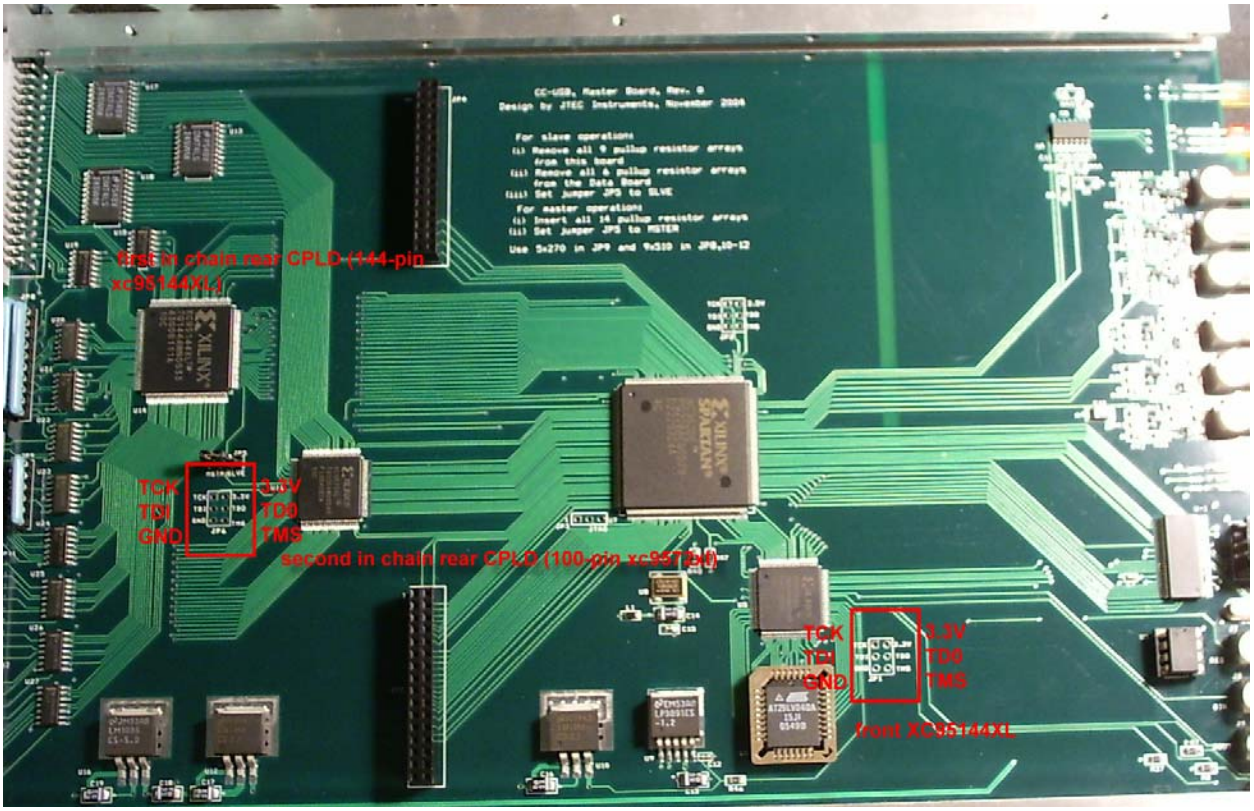
CPLD files for CC-USB upgrade Broadcast (04/19/2006):

1. **cc-atmmgr_flash_040306** - for the front XC95144XL; manages programming of flash memory.
2. **cc_lammgr_brdcst_041906** - for the first in chain rear CPLD (144-pin xc95144XL).

3. cc_datamgr_021905 - for the second in chain rear CPLD (100-pin xc9572xl).

B1.1: Component side (to be used for older versions with header, remove slot 24)





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3. **cc_datamgr_021905** - for the second in chain rear CPLD (100-pin xc9572xl).

B2) Hardware Release 1.0.b delayed FPGA Booting (10/14/2006)

Delayed booting of the FPGA to give the USB controller time to get ready. The JTAG ports can be accessed after removing the right panel:

File: cc_atmmgr_101406.jed

The 3x2 header footprint closest to the front - close to the bottom

Front of the module <- VCC --o o-- TCK
TDI --o o-- TDO
TMS--o o-- GND